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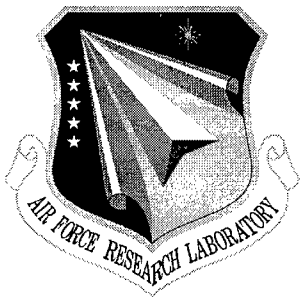


# RELIABILITY-DRIVEN CAD SYSTEM FOR DEEP-SUBMICRON VLSI CIRCUITS

**University of Illinois**

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This report describes development of simulation tools for analysis of ESD protection circuits, part of our reliability-driven CAD system for deep-submicron VLSI/ULSI circuits. Conventional layout extraction tools are inapplicable to ESD protection where parasitic devices and non-standard devices such as SCRs play a large role. We have developed a layout extraction tool which produces input decks for the ESD circuit simulation tool iETSIM. Substrate coupling effects impact the behavior of ESD protection circuits. Herein, we present a circuit-level model for substrate coupling effects and a substrate resistance extraction methodology. We also present an improved, simplified model for semiconductor resistors which has been implemented in iETSIM.

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# Reliability-Driven CAD System for Deep-Submicron VLSI Circuits

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Abstract

This report describes development of simulation tools for analysis of ESD protection circuits, part of our reliability-driven CAD system for deep-submicron VLSI/ULSI circuits.

Conventional layout extraction tools are inapplicable to ESD protection circuits where parasitic devices and non-standard devices such as SCRs play a large role. We have developed a layout extraction tool which produces input decks for the ESD circuit simulation tool iETSIM.

Substrate coupling effects impact the behavior of ESD protection circuits. Herein, we present a circuit-level model for substrate coupling effects and a substrate resistance extraction methodology.

We also present an improved, simplified model for semiconductor resistors which has been implemented in iETSIM.

**Subject Terms: Reliability-driven CAD, EOS/ESD, CMOS integrated circuits**

# Chapter 1

# Overview of Completed Research

Over the past 4 years, with support from Rome Laboratory, we have worked on development of a reliability-driven CAD system for deep-submicron VLSI circuits. We have focused on three reliability issues: hot carrier induced degradation, electrical overstress/electrostatic discharge, and electromigration. Our tool set ranges from an input-pattern-independent reliability rule checker to an electrothermal circuit simulator.

The behavior of a CMOS circuit before and after hot carrier induced degradation may be simulated with ILLIADS-R which is based on the fast and accurate timing simulator ILLIADS. Although ILLIADS is much faster than SPICE (up to three orders of magnitude faster), it is particularly useful for simulation of subcircuits or the critical path, as it is not practical to perform detailed reliability simulation of an entire VLSI chip containing millions of transistors. For full-chip reliability assessment, we have developed iRULE. iRULE obtains a realistic worst case estimate of the transition activity at each node, applies a macromodel for hot carrier degradation, and flags those critical transistors which may suffer significant hot carrier induced degradation. We have also demonstrated that the procedure for automatic high-level synthesis can be specified such that hot carrier induced degradation is minimized

in the final chip. Further details of our work on hot carrier reliability may be found in our 1995 yearly report.

Electromigration reliability is evaluated with iTEM, the Illinois Temperature-Dependent Electromigration Diagnosis Tool. Internal to iTEM is a chip substrate temperature profile simulator named ILLIADS-T. ILLIADS-T considers the power consumption of each gate and the package thermal parameters to create a temperature map of the substrate. The results of ILLIADS-T simulations have been confirmed with physical experiments on a test chip. From the circuit layout, iTEM creates a resistive model of the power and ground bus networks. ILLIADS-T provides the transistor currents which flow into/out of the power bus contacts. Thus, iTEM can calculate the current density in every segment of power bus interconnect. Interconnect temperature is estimated by considering heat flow to the substrate and Joule heating in the line. The electromigration mean-time-to-failure is estimated based on current density and temperature using a modified Black's equation. iTEM was documented in our 1996 yearly report and ILLIADS-T in the 1997 report.

iETSIM, the Illinois Electrothermal Circuit Simulator, is a SPICE-like tool intended for verification and optimization of ESD protection circuit designs. The device models extend to the breakdown region and contain temperature dependent parameters. The simulator simultaneously solves for the temperature and currents of the devices in the circuit. Thus, the point of thermal runaway (catastrophic failure) can be identified by iETSIM. iETSIM has been verified through several studies of industrial protection circuits in which experimental and simulation results were compared. This work is described in the 1996 and 1997 yearly reports.

A layout extraction tool iLEX has been developed to automatically generate input

decks for iETSIM based on the circuit layout. iLEX extracts both the intentionally designed protection devices and the parasitic devices (diodes, BJTs, etc.) which may turn on during an EOS/ESD event. iLEX is described in chapters 2 and 3 of this report. Chapter 4 contains a description of a new semiconductor resistor model (and parameter extractor) which has been implemented in iETSIM.

# Chapter 2

# Layout Extraction and Verification for CMOS I/O Circuits

## 2.1 Introduction

Protection circuits for chip I/O's often incorporate parasitic devices and the layout of these devices does not conform to normal design rules [1][2]. Layout extraction is critically important for design validation since it provides a link between layout and circuit analysis. The traditional emphasis of computer-aided design has been on the chip core circuitry, whereas the design and layout of I/O cells have relied heavily on design expertise and guidelines. Thus, commercial layout extraction programs are only capable of performing limited extraction and verification of the I/O layout. The limitations of commercial extraction tools stem from the following.

- They perform device extraction based on *Boolean* operations of layout masks. Only resistors and diodes marked by specific device layers are identified [3]. The tools can not extract SCRs or parasitic devices such as field transistors and parasitic BJTs. Note

that the parasitic devices may be an integral part of the protection circuit or may be an unintended result of the layout, not recognized by the designers. In any case, they may play an important role during ESD stress events.

- Commercial extractors provide the circuit schematic under normal operating conditions, i.e., when the chip is powered up. However, the circuit is typically not powered during ESD events. An ESD event can generate stress current in excess of 1 A. The normal device models may not be applicable because devices are operating in high current regimes or are biased differently from normal operating modes. Therefore, the schematic for circuit simulation must be determined according to the ESD stress condition.

Thus, we present a new layout extraction program iLEX (*i*llinois *L*ayout *EX*traction for CMOS I/O circuits) [4][5][6]. The program extraction flow is outlined in Fig. 2.1. The program takes layout input in CIF or GDSII format and generates the input decks for the circuit simulator iETSIM. The extraction program consists of three major parts:

- **Device Extraction**: A generic device extraction approach is employed to extract all devices used in I/O circuits.

- **Stress Annotation**: Given a specified ESD stress condition, the device bias conditions are identified and the circuit schematic is extracted. The ESD stress condition is defined by specifying an I/O pad zapped positively or negatively with respect to another pad ($V_{dd}$, $V_{ss}$, or any other I/O pad).

- **BJT Extraction**: The program extracts parasitic BJTs and detects *critical* ones. A critical parasitic BJT is defined as a BJT which is an unintended byproduct of the

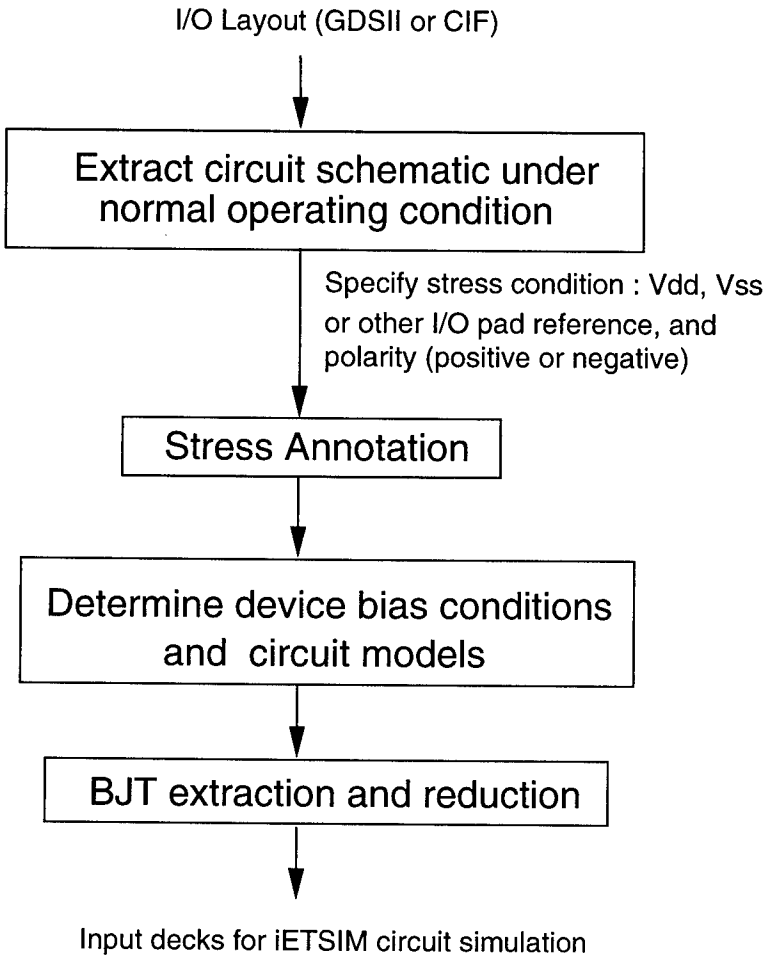


Figure 2.1: The iLEX extraction flow diagram.

layout. A critical BJT's turning-on can induce circuit failures.

## 2.2 Intermediate Representation

In this section, we present an intermediate representation used to support extraction. The representation is designed to be generic. The typical representation of a VLSI layout is the geometrical description of masks. In CIF format, the mask is described by a set of polygons or wires per layer which specify the opaque regions. However, additional abstractions besides the geometrical description are needed for extracting complex device structures. The general structure of a circuit can be mapped into the hierarchical form shown in Fig. 2.2. A circuit

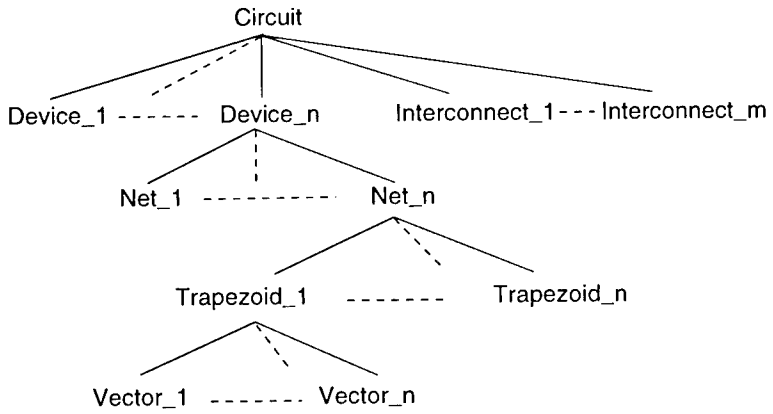


Figure 2.2: The hierarchical representation for a circuit.

contains devices and interconnect nets. A device is made up of a set of nets. A net is composed of connected trapezoids, and vectors make up the trapezoids. The hierarchy represents the layout at different abstraction levels. Vector and trapezoid belong to the geometrical domain. Net is the structural representation. Device and circuit are functional abstractions. Such a hierarchical representation is geometry-conserving. In other words, the geometrical information for any level of abstraction is retained throughout the hierarchical

structure. In addition, the objects in the hierarchy contain pointers to their parents. Each object may have multiple parents. For instance, a particular net may belong to several devices. These upward pointers allow the objects to access their high-level abstractions.

The mask layer data must be transformed into new layer representations suitable for device extraction. The diffusion layer, for instance, is derived from three mask layers: active layer, select layer and well layer. We use an edge-based scan line algorithm to perform *boolean* operations on the masks [7][8][9]. As the trapezoid representation is needed for net abstraction, vectors for a polygon are decomposed into trapezoids [9]. The silicon substrate is divided into non-overlapping trapezoids as shown in Fig. 2.3.

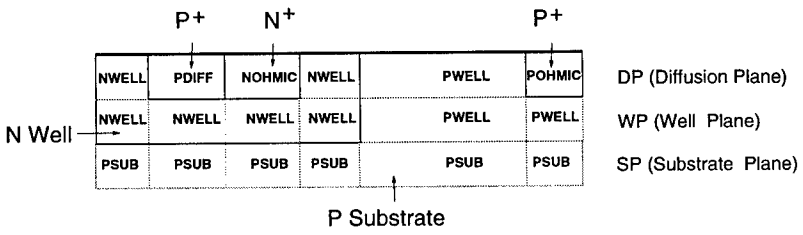


Figure 2.3: Substrate represented by non-overlapping trapezoids.

Connected trapezoids are grouped into nets to provide a structural abstraction for geometrical layout. The scan line algorithm extracts nets according to a *connectivity matrix* which specifies the connectivity relationships between different layers. The device is composed of nets. There are three kinds of nets, namely *substrate net, interconnect net,* and *contact net.* An interconnect net is a set of connected interconnect layer trapezoids. The substrate net is composed of adjacent substrate layer trapezoids of the same kind.

The extraction of contact nets is handled differently from interconnect nets and substrate nets, because contacts do not abut each other. Contacts which are connected to the same substrate and the same interconnect net make up one contact net. In Fig. 2.4, there are two

substrate nets Sub1(NDIFF) and Sub2(POHMIC) and three interconnect nets Inter1, Inter2

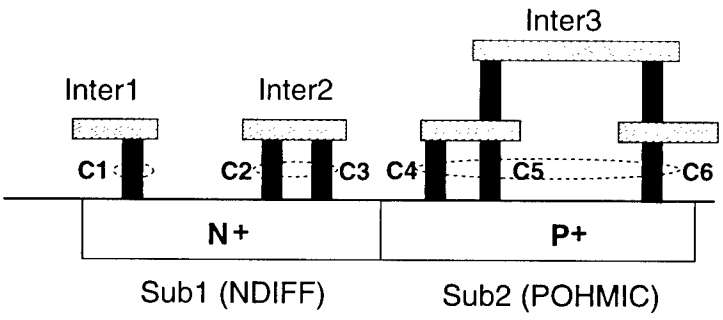


Figure 2.4: Extraction of contact net.

and Inter3. Three contact nets, which are denoted by dashed circles, are extracted, namely CN1, CN2 and CN3. CN1 consists of C1. CN2 is composed of C2 and C3. CN3 consists of C4, C5, and C6.

## 2.3 Device Extraction and Layout Verification

Based on the proposed structural representations of the layout, we developed a generic device extraction technique. The device extraction concept is also extended to I/O layout verification. In addition, cluster extraction of devices and subcircuits is performed to simplify the circuit schematic.

### 2.3.1 Device extraction

To help explain the device extraction approach, we introduce the concept of a *device graph* (DG). Each device graph is used to describe a type of device. The basic structure of the device graph is defined as $DG = (N, R, s)$, where $N$ is the set of nets in the device, $R$ represents the set of relationships between the nets, and $s$ is the *seed* net of the graph. The

relationships in $R$ can be categoried as below

- R1: Adjacency
- R2: Electrical connectivity
- R3: Geometrical position

The device graph proposed in this work is more general than the one in [10] introduced for analog bipolar verification. Figure 2.5 depicts device graphs for PMOS transistor (the extraction of well contacts is necessary for the PMOS device model covering the snapback regime) and n-diffusion resistor. In graphical notation, a net is represented by a filled circle, and multiple nets by double circles. A solid line or dashed lines indicate the adjacency relationship between two nets. A contact net is connected with dashed lines when it is considered optional. The seed net is marked by an arrow. It is the location from which the DG can be constructed by the breadth-first neighbor searching.

MOS transistors and diffusion resistors can be completely specified with the adjacency relationship R1. However, for identification of other types of devices, specifications for R2 and R3 are necessary. The device graph for the thick field device (TFD) is illustrated in Fig. 2.6. R2 specifies that nets N2 and N3 can not be at the same electrical potential, and they can not belong to one MOS transistor if they are associated with MOS transistors. In addition, either of the two interconnect nets connected to N2 or N3 must be exposed to ESD stress. R3 specifies that the distance between net N2 and N3 must be less than or equal to 2 $\mu m$. The distance is process technology dependent. The device graph for an LVSCR (low-voltage triggered SCR) is given in Fig. 2.7. The LVSCR is a commonly used protection device in deep submicron CMOS technologies [11].

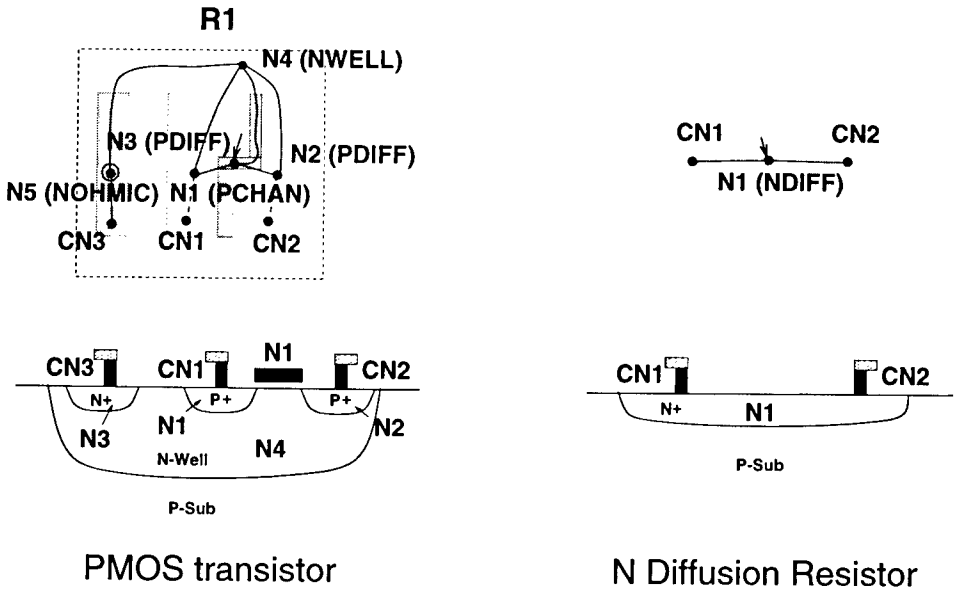


Figure 2.5: Device graphs for the PMOS transistor and the n-diffusion resistor.

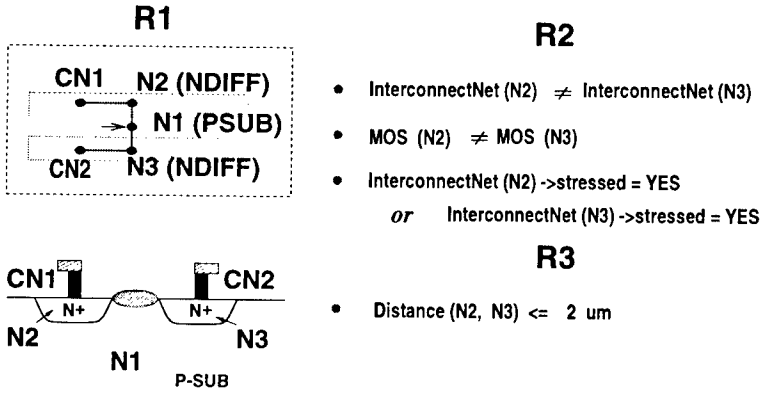


Figure 2.6: Device graph for the thick field device.

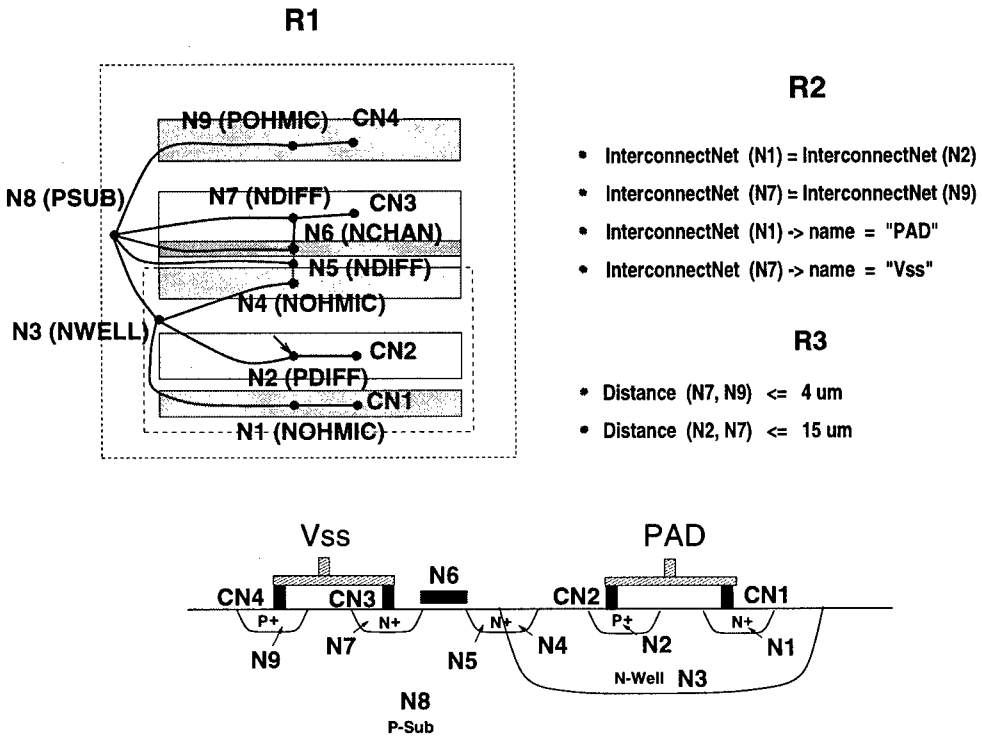


Figure 2.7: Device graph for LVSCR.

Using the device graph, the extraction is performed as following.

1. Identify the device's seed net by its type.
2. Construct the DG by following R1.
3. Check R2.
4. Check R3.

The specification of the seed net facilitates matching a device graph with layout. The matching procedure is aborted at any step when a device graph can not be constructed. With the device graph, the extraction of a new device can be easily implemented by calling generic functions supported by the extraction framework.

### 2.3.2 Layout verification

Normal design rules can often be described by using geometrical relationships between mask layers. However, I/O layout does not conform to normal design rules. A different set of rules are often developed for I/O circuits [2]. The descriptions of I/O rules often involve specification of layout geometries associated with layout structures and electrical circuit properties. Limited I/O layout verification using commercial tools often make extensive use of user-defined marking layers. This requires that circuit designers and layout engineers have in-depth understanding of protection circuits. Still, the majority of I/O design rules can only be checked by expert's visual inspection. I/O rules may not be fully verified in industrial products because of the lack of CAD tools.

With the device graphs, I/O design rule checking can be easily performed by searching

for *error devices.* The design rules are described by error device graphs. The error device graph for a latchup path can be defined similarly as the DG for an SCR. The detection of an error device will signal a design or layout error. Layout verification using device graphs can check the design rules described by both electrical and geometrical properties. Typical I/O rule examples are guard ring rules and driver contact rules (the contact-to-gate spacings for protection devices are often more than the minimum spacing) [2]. Most of the I/O rules can be checked by detecting error devices. One exception is the parasitic BJT detection. The detection of critical parasitic BJTs is very important for I/O verification. However, it requires knowledge of ESD stress conditions (dynamic verification as opposed to static verification using device graph concept). Thus a different treatment is needed. The BJT extraction method will be described later.

### 2.3.3 Cluster extraction

Extracted I/O circuit schematics can often be simplified by clustering devices. For example, merging of multifinger MOS transistors into a single MOS transistor results in a simplified circuit topology and thus faster electrical simulation. The collection of same type devices with identical *device signature* is extracted as a *device cluster.* We define the device signature by a set of its associated interconnect net IDs. The clustering process is straightforward and performed by comparing device signatures. Similarly to device clusters, clustering can also be done at the circuit level. Subcircuits form a subcircuit cluster after clustering. A subcircuit's signature is defined similarly as for the device. In Fig. 2.8, the circuit schematic of a typical output protection circuit is simplified by performing device clustering and subcircuit clustering. Clustering can not only facilitate device reduction but also identify critical devices

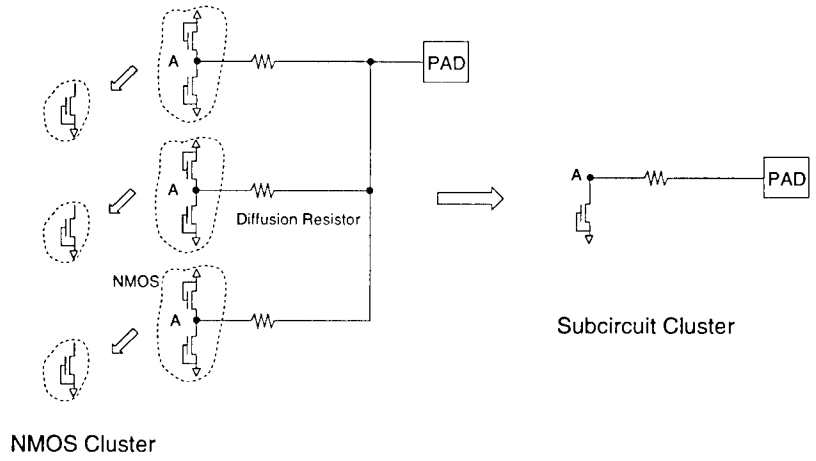


Figure 2.8: An example for device cluster and subcircuit cluster. All nodes labeled A are assumed to be at the same electrical potential.

among peers as will be discussed later.

## 2.4 Stress Annotation

Under ESD testing the chip is not powered up. According to the MIL Standard 883C method 3015.7 [12], a Human Body Model (HBM) test should zap all possible pin combinations of a chip for both positive and negative stresses, and the chip must pass 2 kV HBM-ESD level for all stresses. When the ESD zapping is performed between two pads, all other pads are kept floating. Considering an I/O cell, it must pass the required protection level with respect to $V_{dd}$, $V_{ss}$ and any other pad for both polarities.

Since the behavior of a device is bias-dependent, its circuit model can only be determined according to its operating condition. We propose a static analysis technique, called *stress annotation*, to determine each device's applicable circuit model. Figure 2.9 illustrates the stress annotation performed on an I/O circuit for a specified stress condition, i.e., positive

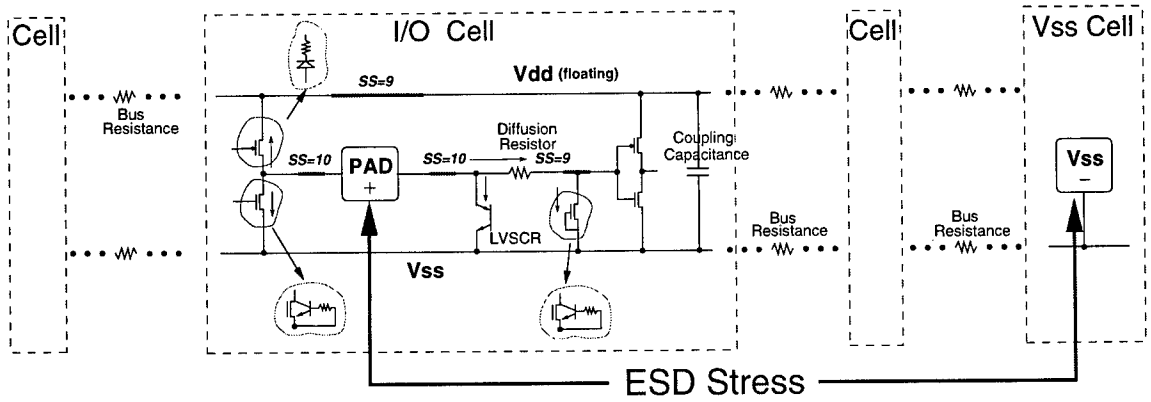


Figure 2.9: The stress annotation to identify the device's bias condition, and determine its circuit model. The PMOS transistor is substituted with a diode and a resistor. The NMOS transistor is replaced by a high current model covering the snapback regime.

stress on the pad with respect to $V_{ss}$. First, the circuit schematic for the layout at the normal operating condition is extracted. Then, the stress annotation is conducted using a breadth-first search to propagate the stress current from the stressed pad. The stress current passes through forward-biased pn junctions and resistors. The search stops when a reverse-biased pn junction is reached. Each interconnect net in the current path is annotated with its *stress strength* (SS). The relative voltage levels between two interconnect nets can be compared by checking their stress strength. Thus, stress annotation will help identify parasitic BJT devices, which will be discussed in the next section. Starting with an initial value, such as 10 used in Fig. 2.9, the stress strength is reduced by one whenever the stress current passes a resistive device.

Following the stress annotation, each device's circuit model will be determined. When a device is under ESD current stress, a high current model must be used, such as an NMOS model which covers the snapback regime [13] or a resistor model which includes velocity saturation [14]. When a pn junction in a transistor is forward-biased, it operates as a diode

instead of as a transistor. The junction formed between the drain diffusion of the driver PMOS transistor and the n-well is forward biased. As a result, the n-well is charged up and the high current is propagated to the $V_{dd}$ power line via the well contact. Therefore, we may substitute the PMOS transistor with the serial combination of a forward-biased diode and a well resistor. This is the applicable circuit model for the PMOS transistor under this specific bias condition.

## 2.5 BJT Extraction

In this section, we present a systematic approach to identify potentially conducting parasitic BJTs.

### 2.5.1 Lateral BJT extraction

Ideally, the ESD current should be conducted through intentionally designed protection devices such as TFDs, LVSCRs or NMOS transistors. However, parasitic BJTs are often the side effects of layout or design. The turn-on of lateral BJTs is a cause of chip ESD failures [1][15][16][17]. Any two diffusions or wells can potentially form a BJT. Hence the total possibilities for BJTs can be $2\binom{n}{2}$, where n is total number of diffusions or wells within a single cell, $\binom{n}{2}$ denotes the possible number of pairs and the constant 2 accounts for both polarities (positive and negative). However, with the device bias conditions and relative potentials from the stress annotation, the number of BJTs which need to be included in the simulation deck can be greatly reduced. An example of parasitic BJT identification is shown in Fig. 2.10. Once the stress annotation has been performed, the forward-biased pn

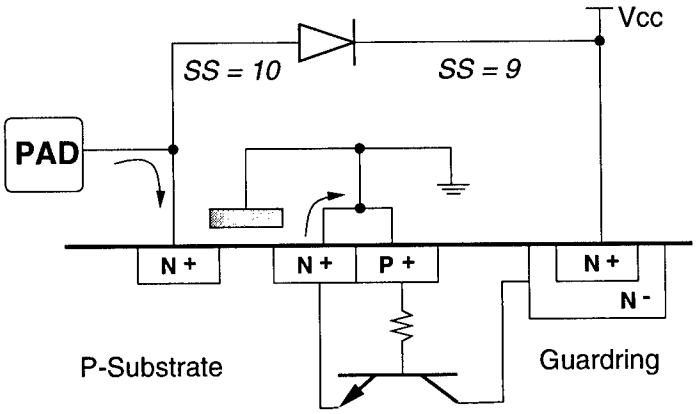


Figure 2.10: Extraction of lateral parasitic BJTs. The source of NMOS transistor (emitter) and guard ring (collector) form a parasitic BJT.

junctions are identified as possible emitters of BJTs. Those diffusions or wells which are stressed with high voltages are identified as possible collectors (checking the lower voltages for the extraction of lateral PNPs). Note that different BJTs will be extracted for different stress conditions. If there are $p$ emitters and $q$ collectors, the number of possible BJTs is $pq$. However, not all of them will conduct significant currents. Therefore, further reduction is needed to detect critical BJTs among them. The gain $\beta$ of parasitic BJT is the most important parameter in a BJT model. Hence, it is used as a criterion for reduction. $\beta$ is inversely proportional to the square of the base width $W$. The set of reduction rules is listed below while the referenced configurations are illustrated in Fig. 2.11.

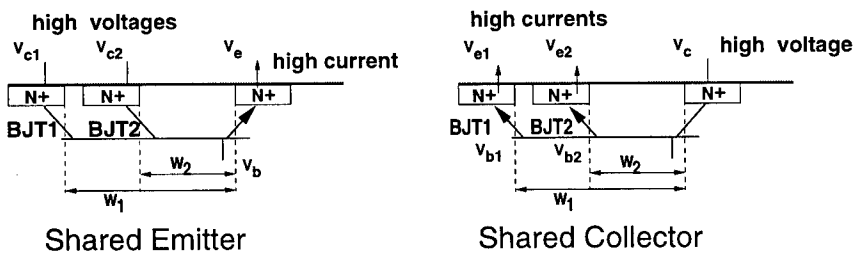


Figure 2.11: Configurations of parasitic BJTs for reduction.

1. Shared emitter rule:

   (a) If $V_{c1} \leq V_{c2}$, and $\beta_1 < \beta_2$, remove BJT1.

   (b) If $V_{c1} < V_{c2}$, and $\beta_1 \leq \beta_2$, remove BJT1.

   (c) Otherwise, no reduction.

2. Shared collector rule:

   (a) If $V_{e1} \geq V_{e2}$, and $\beta_1 < \beta_2$, remove BJT1.

   (b) If $V_{e1} > V_{e2}$, and $\beta_1 \leq \beta_2$, remove BJT1.

   (c) Otherwise, no reduction.

3. Minimum $\beta$ rule (technology dependent):

   - If $\beta < \beta_{threshold}$ ( $W > W_{threshold}$ ), no BJT.

Note that the reduction rules consider $V_c$. To first order, collector current is independent of the value $V_c$. In the shared emitter configuration, there exist two current paths, from C2 to C1 then to the shared emitter, or from C2 to the emitter. $V_{c1} < V_{c2}$ and $\beta_1 \leq \beta_2$ indicates that the path from C2 to the emitter is less resistive, so that the current is shunted through $C_2$. The minimum $\beta$ rule is technology dependent and the value can be specified by users.

### 2.5.2 Vertical BJT extraction

Vertical BJTs can also impact ESD circuit performance. Current injected by vertical BJTs into the substrate will raise the substrate potential and may change the substrate bias of other devices. When a diffusion in a well is forward-biased, a vertical BJT will be extracted under

either of two situations, i.e., the diffusion is at high potential while the substrate is grounded, or the diffusion is grounded while the substrate is under negative stress. For example, the diode in Fig. 2.9 is replaced by the vertical BJT Q1 as shown in Fig. 2.12. The lateral BJT Q2 formed by the drain and source of the PMOS transistor is extracted according to the

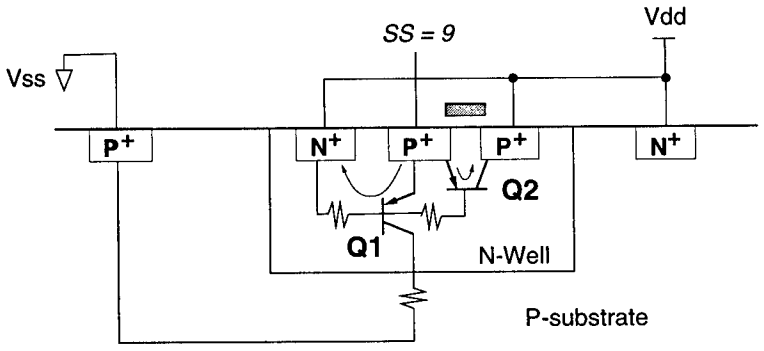


Figure 2.12: BJTs formed by the PMOS transistor.

lateral BJT extraction method. There are two current paths from PMOS drain diffusion to $V_{dd}$, i.e., through Q1 and Q2. Although Q1 (base emitter diode) is the intended protection device, Q2 may conduct a significant amount of current if the well resistance is high [18]. If the size of PMOS transistor is narrow and can not sustain the ESD current, circuit failure will occur.

## 2.6 Walk-Through Examples

Three industrial layout examples from the literature are used to illustrate the iLEX extraction methodology. Also, we will show that the extracted circuits and the simulated results agree with the reported experiments.

### 2.6.1 An input protection circuit

An input protection circuit typically contains a primary protection device and a secondary protection device. The secondary protection is used to protect the gate oxide of the input transistors; the secondary device is often a gate-grounded NMOSFET (GGNMOS). The circuit in Fig. 2.13 uses a thick field device (TFD) as the primary protection and a diffusion resistor as the drain isolation. Two different layouts for the input protection circuit are shown in Fig. 2.13. Although both layouts have the same circuit schematic under normal

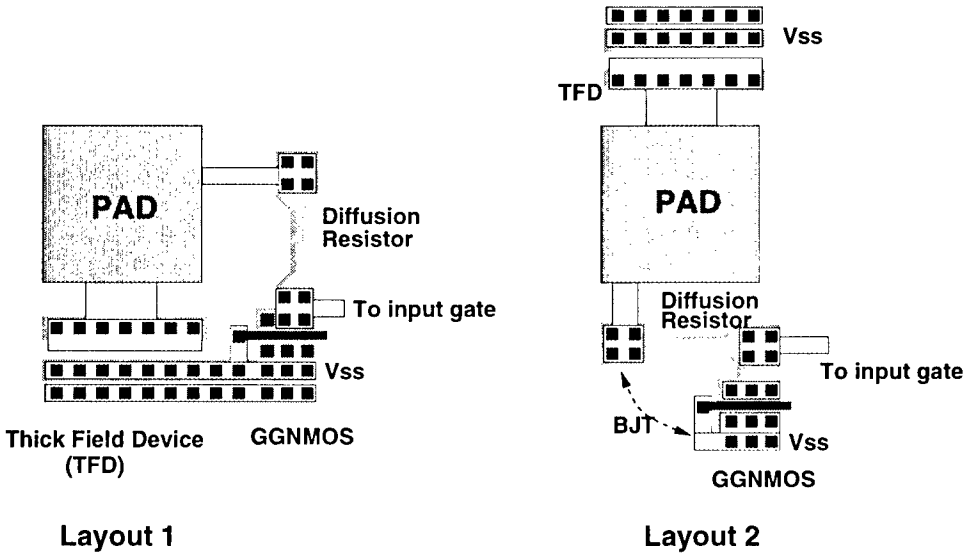


Figure 2.13: Two different layouts for a two-stage input protection circuit.

operating conditions, it has been found experimentally that there exists a lateral parasitic BJT in layout 2 under positive stress on the pad w.r.t. $V_{ss}$ [15][19]. Now we will analyze the two layouts using the iLEX methodology. The layouts and extraction details are shown in Fig. 2.14 and Fig. 2.15. The circuit nodes in the device graphs are numbered on the layouts. A lateral BJT is denoted by the node numbers of its collector and emitter. For example, (1,

2) represents the BJT formed by node 1 as its collector and node 2 as its emitter.

First, the stress annotation is performed on the circuit schematic. Since the drains of the TFD and GGNMOS are under positive stress, the high current models which include the bipolar action must be used. Next, the BJTs are extracted for the two layouts as described below.

- *Layout 1 :* As shown in Fig. 2.14, diffusion 2 is forward-biased after the GGNMOS is triggered, while diffusions 1, 3 and 4 are under high voltage stress. Therefore, three lateral BJTs may be formed. They are denoted as (1, 2) (3, 2) and (4, 2). To perform the BJT reduction, BJTs (4, 2) and (1, 2) are clustered to form the shared emitter configuration. BJT (4, 2) is eliminated according to the shared emitter rule. Since BJTs (3, 2) and (1, 2) are already included in the TFD and NMOS high current models, **no extra parasitic BJT exists for layout 1.**

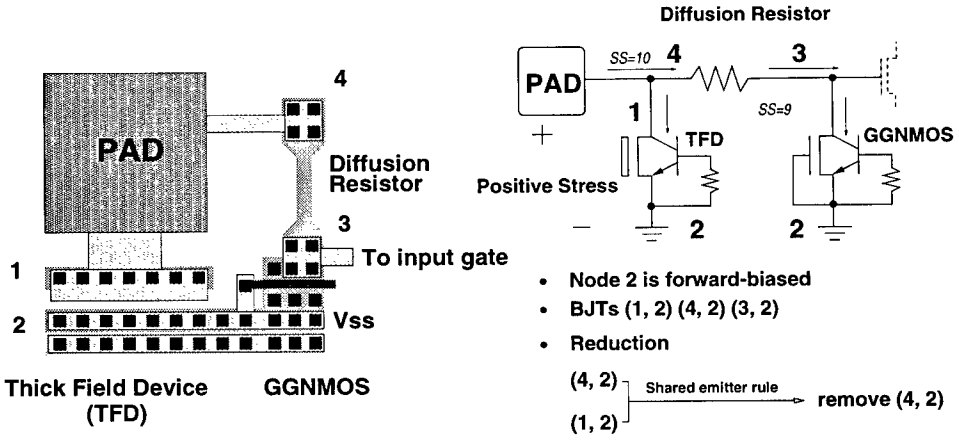


Figure 2.14: Analysis of layout 1.

- *Layout 2 :* As illustrated in Fig. 2.15, diffusions 2 and 5 are forward-biased. Since diffusions 1, 3 and 4 are stressed with high voltages, there are six possible lateral

BJTs, namely (1, 5) (4, 5), (3, 5), (1, 2), (4, 2) and (3, 2). The BJTs are reduced similar to layout 1. The TFD and NMOS high current models include BJTs (1, 5) and (3, 2), but **parasitic BJT (4, 2) is detected for layout 2.**

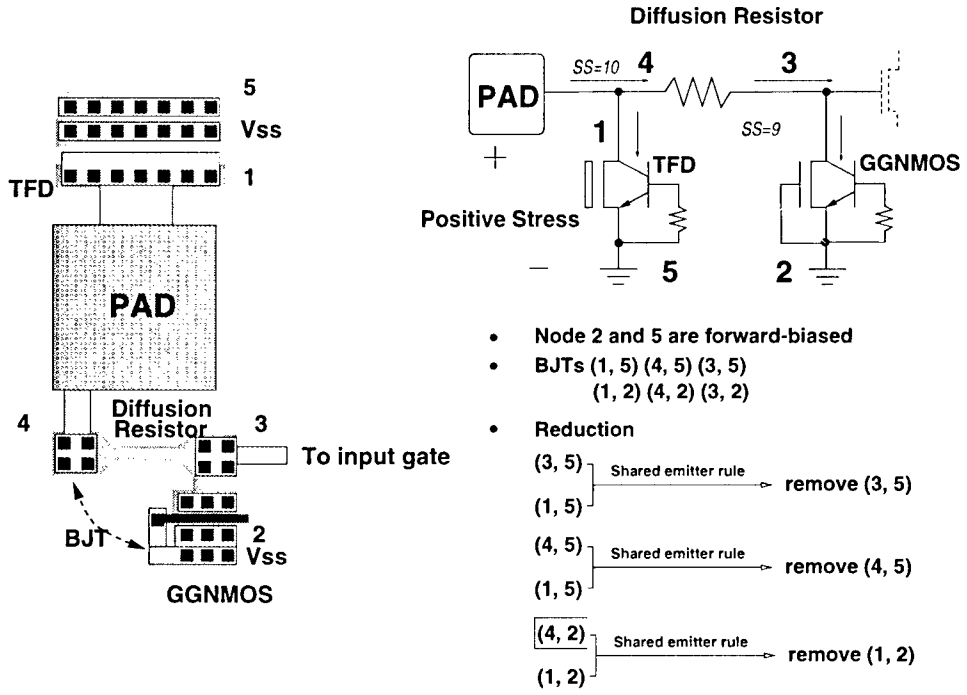


Figure 2.15: Analysis of layout 2. Lateral BJT (4, 2) is detected under the positive stress to pad w.r.t. $V_{ss}$.

### 2.6.2 An input protection circuit – II

The second example is also an input protection circuit. The circuit layout and details of extraction are shown in Fig. 2.16. It uses an LVSCR instead of a TFD as the primary protection device. Although the circuit schematic is similar to the one in the previous example, the circuit failure mechanism is different. The failure site when the pad is stressed negatively with respect to $V_{dd}$ is circled on the layout [16]. It indicates that a parasitic BJT

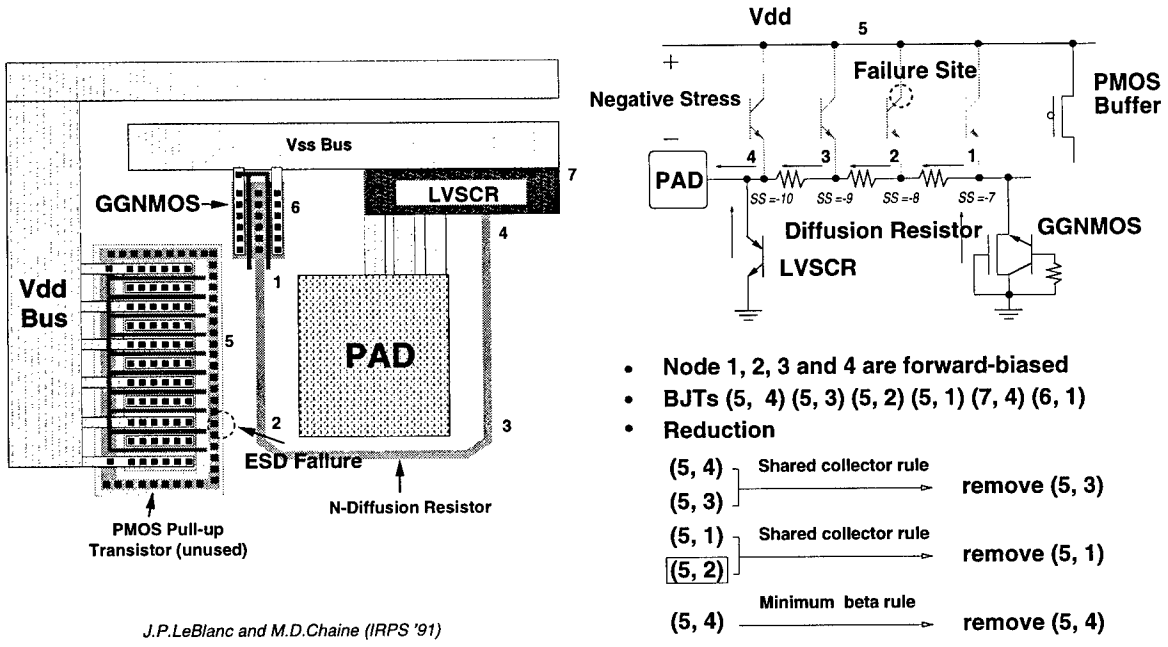


Figure 2.16: Analysis of the input protection circuit – II. Node 7 is the cathode of LVSCR. Since BJT (7, 4) is modeled in LVSCR and BJT (6, 1) is included in NMOS model, BJT (5, 2) is detected as a critical BJT.

(5, 2) turns on and collector failure occurs.

To perform the stress annotation, the negative current is propagated from the pad. The GGNMOS is now stressed negatively. The drain becomes the emitter of its associated BJT. Under negative stress conditions, the diffusion resistor to substrate np junction is forward-biased. We divide the diffusion resistor into three segments. The n-well denoted by node 5 is at high potential. Therefore, there may exist six BJTs (5, 4) (5, 3) (5, 2) (5, 1) (7, 4) (6, 1). After the reduction process, BJT (5, 2) is detected as the critical parasitic BJT. Circuit simulation can now be performed.

### 2.6.3 An I/O protection circuit

The final example illustrates the extraction of vertical BJTs and its importance of including these devices in the simulation deck. The circuit is composed of a gate-coupled NMOS device (consisting of an NMOS transistor, a capacitor and a resistor) and a lateral diode connected to $V_{dd}$ [22]. The circuit schematic is extracted for the case of positive stress on the pad with respect to $V_{ss}$. After we have performed the stress annotation, we proceed to extract lateral BJTs and perform reduction as shown in Fig. 2.17. The procedure stops when there exist no more parasitic lateral BJTs for this specific stress condition. Finally, we extract the vertical BJTs. As the pn junction in the lateral diode is forward-biased and resides in the n-well, the diode is replaced by a vertical BJT.

In Fig. 2.18, we show the circuit simulation results for a 500 mA current stress [21]. Circuit simulation using iETSIM is performed assuming 100 nF chip capacitance $C_c$. The gain of the vertical BJT is low and most of the stress current flows through the base contact to charge $C_c$. Under ESD stress conditions, the capacitance charges up quickly, and the

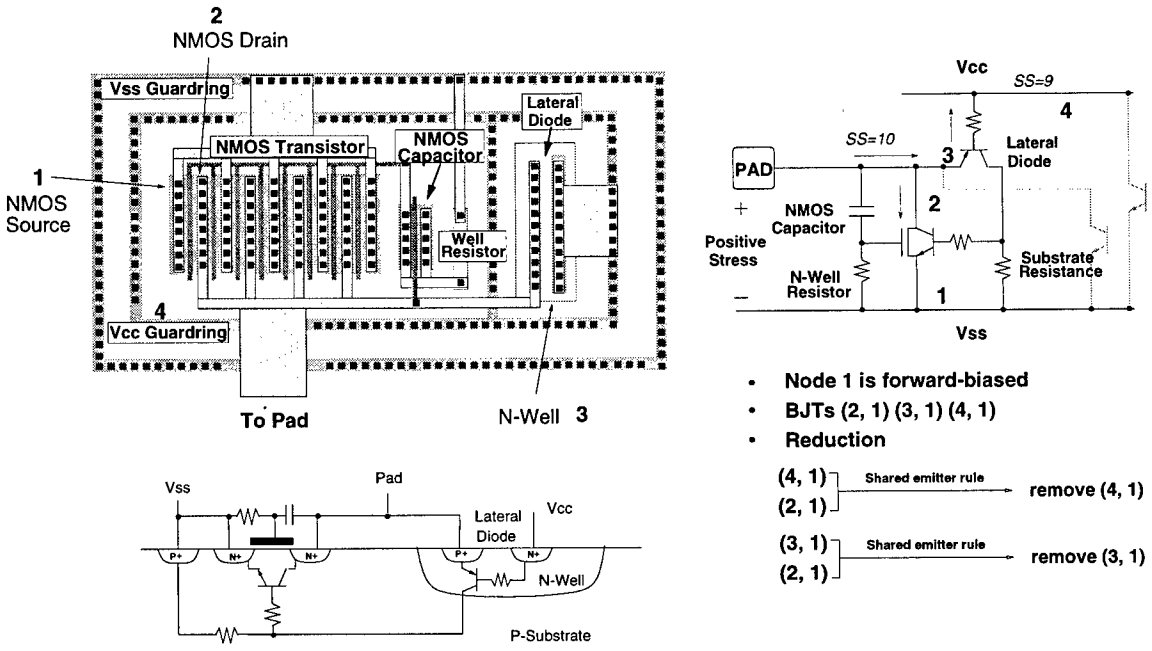


Figure 2.17: Analysis of the I/O protection circuit. Since lateral BJT (2, 1) is included in NMOS snaps back model, no parasitic lateral BJT is detected.

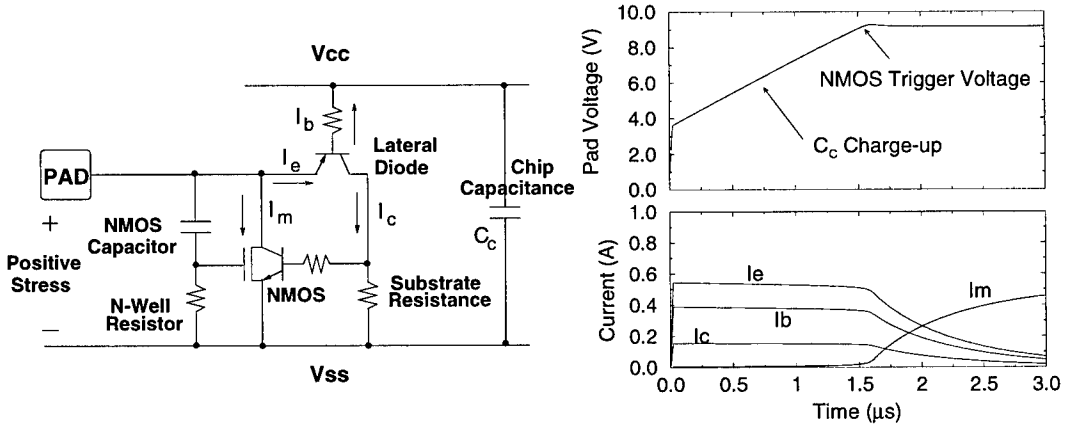


Figure 2.18: Simulation results for the I/O protection circuits under positive stress.

NMOS transistor triggers to conduct the stress current. Note that the collector current of the vertical BJT raises the substrate potential which reduces the trigger voltage of the NMOS transistor.

Finally, the extraction results for the above three examples are summarized in Table 2.1. In summary, the BJT extraction procedure involves three major operations, namely device clustering, stress annotation and BJT reduction. As one can see from the table, each step can greatly reduce the number of BJTs, and eventually pinpoints the critical ones. By using the proposed systematic procedure, we can automatically extract the I/O circuits for full ESD analysis. The extracted results of all above three examples have confirmed the experimental results reported in the literature.

| Circuit Layout | Stress [1] Condition | No. of Lateral BJTs | | | | No. of Vertical BJTs | | |
|---|---|---|---|---|---|---|---|---|
| | | (-, -, -) | (c, -, -) | (c, a, -) | (c, a, r) [2] | (-, -, -) | (c, -, -) | (c, a, -) |
| Ex1 (layout 1) | $V_{ss}$ (+) | 12 | 12 | 3 | **0** | 0 | 0 | **0** |
| Ex1 (layout 2) | $V_{ss}$ (+) | 20 | 20 | 6 | **1** | 0 | 0 | **0** |
| Ex2 | $V_{dd}$ (−) | 42 | 30 | 6 | **1** | 6 | 1 | **0** |
| Ex3 | $V_{ss}$ (+) | 210 | 42 | 3 | **0** | 4 | 1 | **1** |

**(c, a, r)** stands for (clustering, annotation, reduction). A dash denotes that the corresponding operation is not performed.

[1]The stress is from pad to the reference node.

[2]The number of critical parasitic BJTs. The intentionally designed BJTs are excluded.

Table 2.1: Summary of the BJT extraction results.

## 2.7 Full Chip Frame Extraction

The ESD standard requires the protection level to be verified for the full chip. This is due to the fact that reliable individual I/O cells do not guarantee full chip reliability[1][23]. Therefore, verification using simulation must also be performed at the I/O frame level. We

propose a hierarchical approach for the extraction of the chip I/O frame. First, each I/O cell is extracted once and its intermediate representation as shown in Fig. 2.2 is stored in an object-oriented database [24]. The extraction of the full chip I/O frame only utilizes the interconnect relationships among I/O cells. It identifies the bus architecture and extracts bus resistances and power bus coupling capacitances shown in Fig. 2.9. Then, stress annotation is performed on the extracted I/O frame circuit. The extraction of possible parasitic BJT devices must be done for every two adjacent cells.

## 2.8 Run-Time Analysis

The run-time for the cell extraction is dominated by the scan line algorithm for mask geometric operation and net construction [7]. Therefore, the extraction run-time complexity is $O(NLogN)$ where $N$ is the number of vectors for boolean mask operation, or the number of trapezoids for net operation in an I/O cell. Significant portion of the run-time is consumed by building the adjacent relationships among substrate trapezoids. Such relationships are used to identify the neighbor nets in constructing device graphs. It takes less than 2 seconds to extract the MOSIS I/O pad. Further improvement may be achievable by adopting an almost linear complexity algorithm proposed in [9]. The proposed frame-level extraction will take little time in comparison with the cell extraction since the intermediate representations for I/O cells can be retrieved from the object-oriented database.

## 2.9 Summary

We have presented a novel extraction and verification methodology for CMOS I/O cell. To our knowledge, the layout extractor presented is the first comprehensive layout extractor developed for reliability-driven CMOS I/O design. With short turn-around time, extensive ESD protection circuit simulations can be performed by using our extractor and simulator. Thus, design and layout flaws can be detected before the design and layout are committed to silicon.

# Chapter 3

# Substrate Resistance Network Model and Resistance Extraction

## 3.1 Introduction

Circuit simulation is becoming increasingly important for building in ESD reliability early in the product development cycle. An accurate and computationally efficient circuit model for the silicon substrate is critical for capturing the effects of layout on the ESD level. The

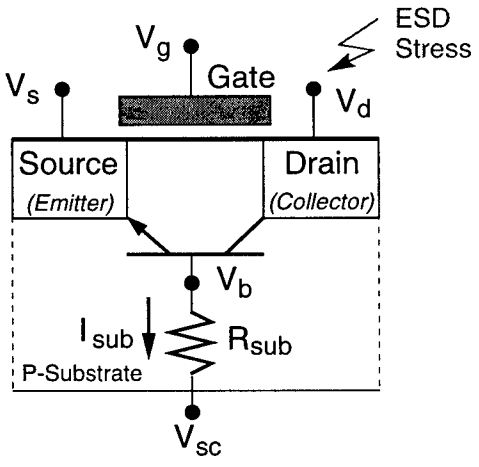


Figure 3.1: Cross-section of an NMOS transistor showing the parasitic NPN transistor and the substrate resistor which connects BJT base ($V_b$) and substrate contact ($V_{sc}$).

substrate resistance is an important parameter because it can determine the on/off state of a device. The limitations of a single resistor substrate model as shown in Fig. 3.1 and used in previous works [13][25][26] are listed below.

- It fails to consider the effects of substrate topside contacts as shown in Fig. 3.2. Each device in the layout can have a different substrate resistance depending on its relative location to the substrate contact. Furthermore, different substrate contacts may be at different electrical potentials. This situation can arise when there is a voltage drop through the metal interconnect path between two substrate contacts.

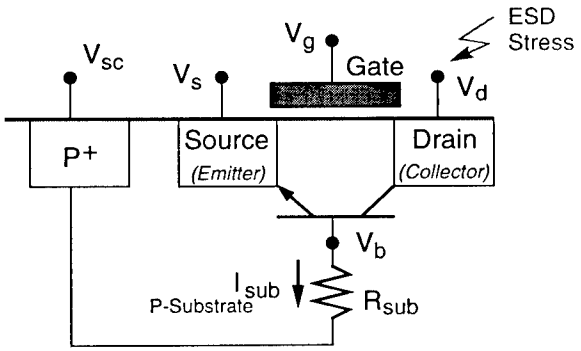


Figure 3.2: Cross-section of an NMOS transistor showing the parasitic NPN transistor and a topside substrate contact.

- It can not model the device interactions through the silicon substrate. Such interactions can significantly affect the circuit's ESD behavior and have been utilized to enhance circuit ESD performance [22][27][28]. On the other hand, circuit failure may occur due to the existence of an unintended substrate current path [1][15][16][17][19][29].

In this chapter, we present a new and general substrate resistance network model and a substrate resistance extractor iSREX (*i*llinois *S*ubstrate *R*esistance *EX*tractor) [30][31].

The model is compatible with the electrothermal circuit simulator iETSIM. iSREX is implemented using the 3D finite difference method. The circuit simulator can be used for protection circuit layout optimization, to detect unintended parasitic current paths, and for failure diagnosis.

## 3.2 Substrate Resistance Network Model

We first present the substrate model for a simple circuit which contains one device, one external substrate injection current and one substrate contact. Next, we demonstrate how to use the model to represent substrate coupling effects in more complicated circuits, including DRAMs.

### 3.2.1 Modeling external current injection

When an NMOS is subject to a positive ESD stress at its drain with $V_g$, $V_s$ and $V_b$ at ground, impact ionization current generated at the drain junction will flow through the substrate resistance and may cause the local substrate potential to rise up and forward bias the source junction. As a result, the parasitic BJT may turn on, causing the NMOS transistor to operate in the snapback regime. Referring to Fig. 3.2, if $V_{sc} \neq 0$, the trigger voltage may be affected. A measured NMOS I-V characteristic is shown in Fig. 3.3. The trigger voltage of the NMOS transistor decreases as the external substrate bias voltage increases. The trigger voltage reduces to the holding voltage when $V_{sc}$ reaches 0.9 V.

CMOS devices residing in the common silicon substrate are also under the influence of substrate currents produced by nearby devices ("external" substrate currents). Such currents can effect a device's local substrate potential. To model the external current injection effects,

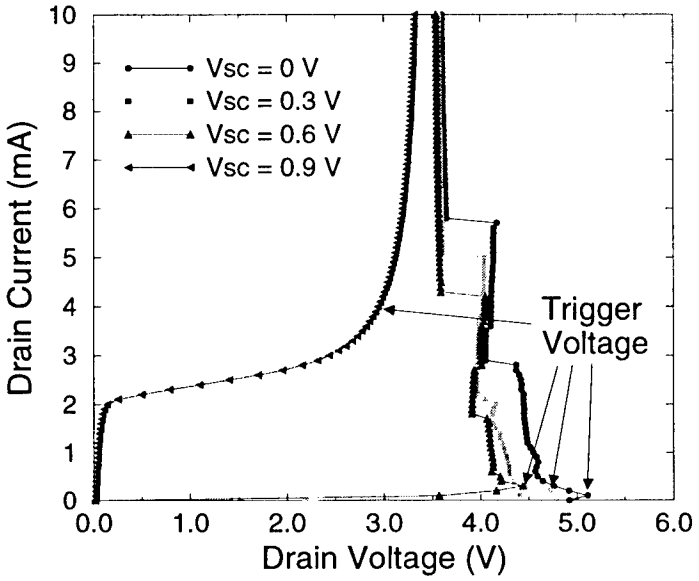


Figure 3.3: The measured I-V characteristics of an NMOS transistor for various substrate bias voltages measured using an HP4145 ($L = 0.25\mu m$, $V_g = V_s = 0$ V).

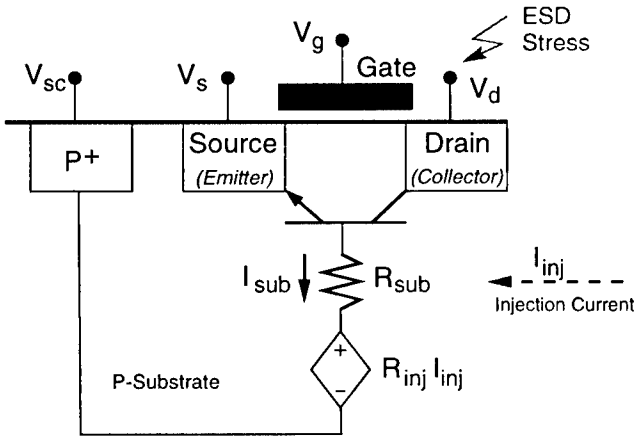


Figure 3.4: The substrate resistance model of an NMOS transistor under the influence of one external current source.

we use the concept of *transfer resistance* [32][33]. It is defined as the surface potential at a point outside the injector divided by the injection current. The substrate resistance model for an NMOS transistor under the injection of current $I_{inj}$ is shown in Fig. 3.4. $R_{inj}$ is the transfer resistance associated with $I_{inj}$. The device local substrate potential due to $I_{inj}$ is modeled by a current-controlled voltage source. By the same token, $R_{sub}$ can be viewed as the transfer resistance due to the impact ionization current $I_{sub}$. Equivalently, resistor $R_{sub}$ can be drawn as a current-controlled voltage source $R_{sub}I_{sub}$. Note that the transfer resistance depends on the relative locations of the injection current source, the substrate contact and the voltage monitoring point.

Although we primarily focus on NMOS transistors in this paper, it is important to note that other kinds of devices are also affected by their local substrate potentials, including parasitic BJTs and parasitic diodes. The corresponding substrate currents are impact ionization currents or base currents of lateral parasitic BJTs, collector currents of vertical BJTs, and forward or reverse currents of parasitic diodes as shown in Fig. 3.5.

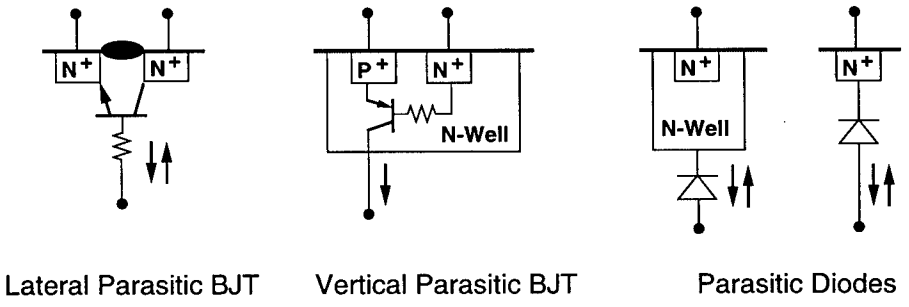


Figure 3.5: Possible parasitic devices under ESD conditions.

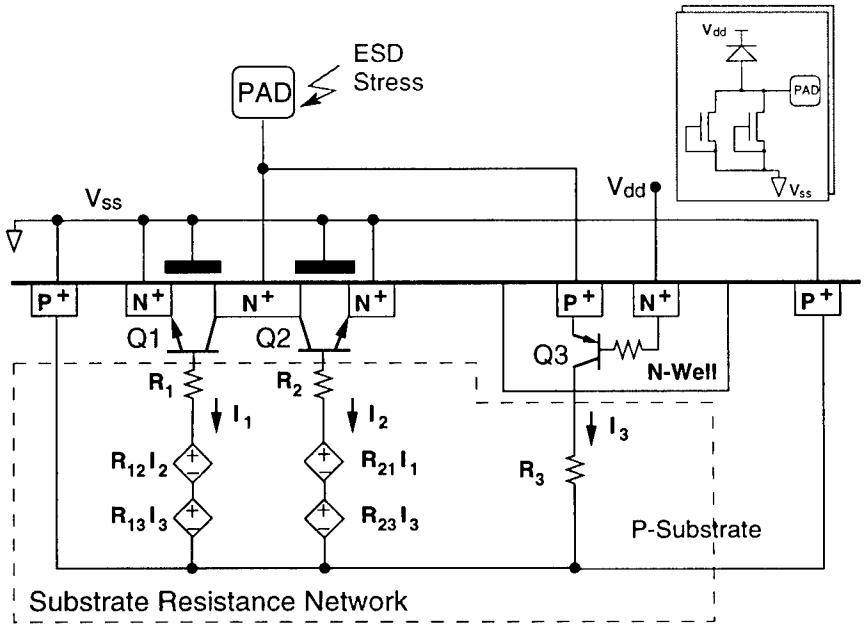


Figure 3.6: The substrate resistance model with multiple substrate current sources.

### 3.2.2 Modeling multiple devices

Figure 3.6 shows an example of a circuit containing multiple substrate current injection sources. The circuit consists of two grounded gate NMOS transistors connected in parallel and a lateral diode to $V_{dd}$. The lateral diode is more generally modeled as a vertical BJT. The substrate contact is a ring structure surrounding the cell layout.

Under positive stress from the pad to $V_{ss}$, there exist three substrate current sources, namely, the impact ionization currents from the collector-base junctions of Q1 and Q2 and the collector current of Q3. Each device's local substrate potential is affected by all devices. These interactions can be modeled by the substrate resistance network shown in Fig. 3.6 inside the dashed lines. Focusing on Q1, its base resistance model consists of three components. $R1$ is the resistance from the base of Q1 to the substrate contacts. The other two components are voltage sources controlled by currents $I_2$ and $I_3$. $R_{ij}$ is the transfer resistance

which can be obtained by dividing the local substrate voltage near the emitter junction of BJT $Q_i$ by the current $I_j$ (other current sources are set to 0). The effect of currents $I_1$ and $I_2$ on the collector voltage of Q3 was neglected in this model, because the collector current of Q3 is primarily controlled by its base current.

The number of voltage sources increases quadratically with the number of current sources. However, the network can often be simplified especially in the cases listed below.

1. The effect of external injection currents on collector voltage of a vertical BJT can be neglected, since the collector current is, to first order, independent of the collector voltage as noted above.

2. Devices of the same kind connected in parallel can be clustered if they are identical, e.g., Q1 and Q2 can be reduced to a single transistor if $I_1 \approx I_2$, $R_1 \approx R_2, R_{12} \approx R_{21}$ and $R_{13} \approx R_{23}$.

3. If a transfer resistance is sufficiently small, the associated voltage source may be omitted (shorted) without affecting the simulation accuracy.

Referring back to Fig. 3.6, if Q1 and Q2 are clustered into a single transistor Q4, the substrate resistance network can be simplified as shown in Fig. 3.7.

With the proposed substrate network model, we can simulate the coupling effects of lateral parasitic BJT in the input circuit drawn in Fig. 2.15. The schematic for simulation is shown in Fig. 3.8 along with a cross-section of silicon substrate. The model parameters for devices such as NMOS transistors can be extracted from the measurements of test structures [20]. Circuit simulation results indicate that there is indeed a significant amount of stress current conducting through the lateral parasitic BJT. The NMOS transistor triggers at 11

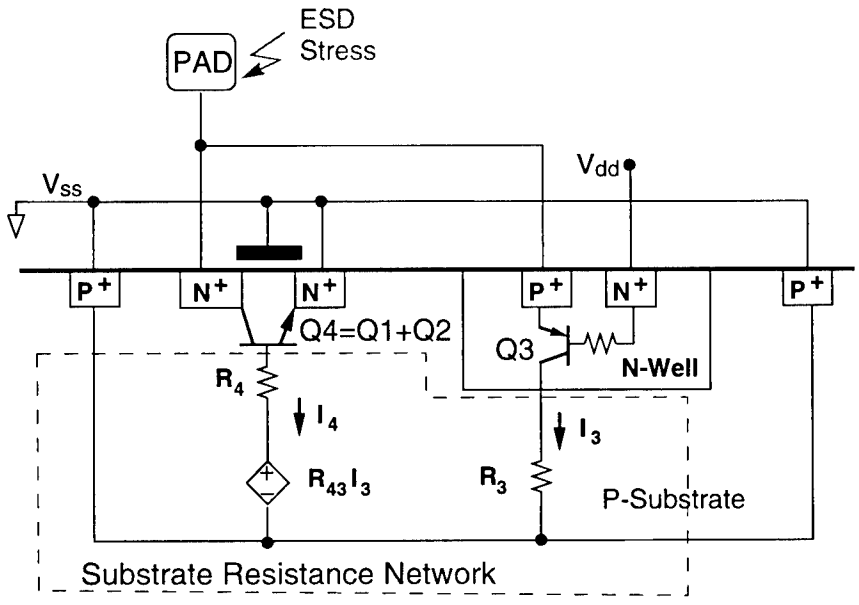


Figure 3.7: The simplified substrate resistance model.

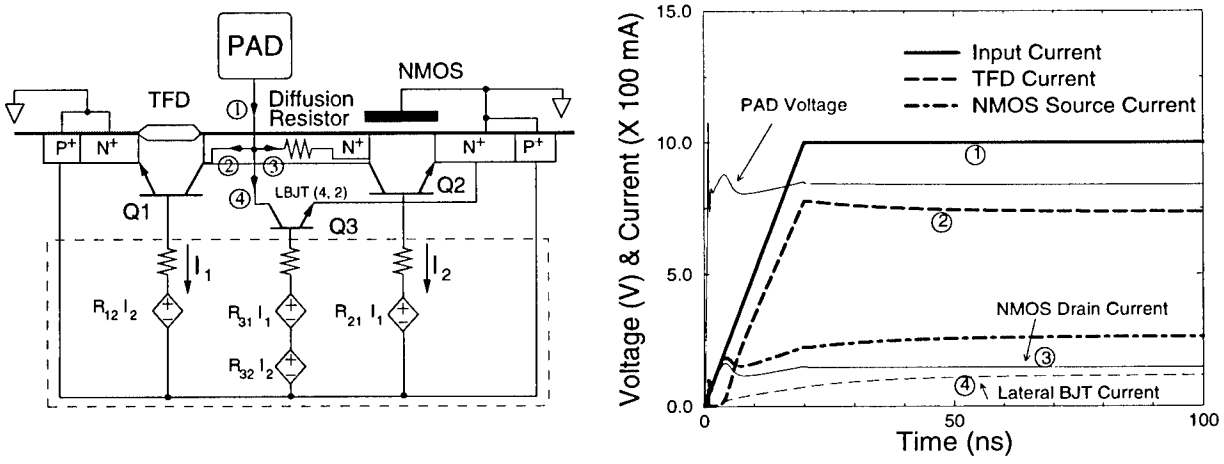


Figure 3.8: The circuit schematic for layout 2 under positive stress and the circuit simulation results.

V and then snapback to its holding voltage 8V. Majority stress current flows through TFD. The NMOS source current is greater than its drain current because part of the source current is collected to the junction connected to pad through lateral BJT (4, 2). This confirms the experimental and failure analysis results reported in [15][19].

### 3.2.3 Modeling multiple substrate contacts

When an I/O circuit layout contains multiple substrate contacts, they may be at different potentials due to the ground bus routing as shown in Fig. 3.9. There exist three substrate contacts in this layout, the two topside contacts $V_{sc1}$ and $V_{sc2}$ and the die backside contact $V_{sc3}$. In general, the three contacts may not have the same potential under ESD conditions, so they need to be modeled as separate nodes in the circuit model. The substrate network

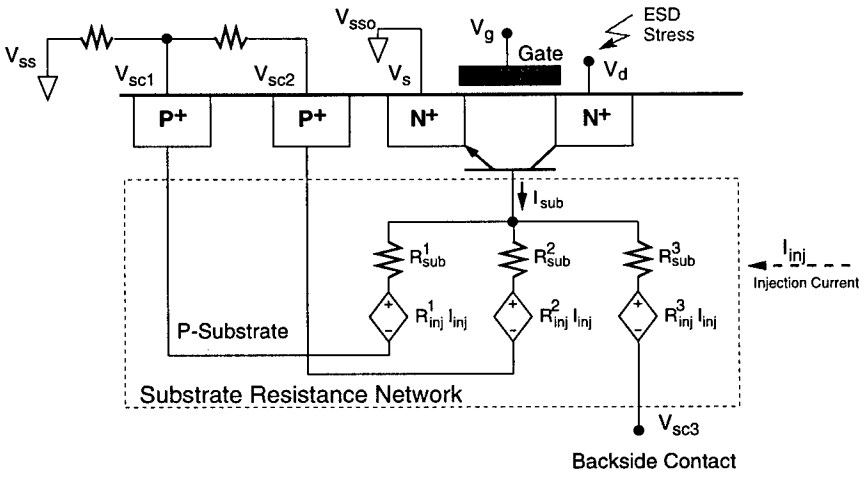


Figure 3.9: The substrate resistance model with multiple substrate contacts.

consists of three parallel branches with each branch having a different reference node. $R^1_{inj}$ is the transfer resistance for current source $I_{inj}$ with reference to node $V_{sc1}$. $R^1_{inj}$ is obtained by dividing the local substrate potential (near the emitter junction) of the NMOS transistor

by the current $I_{inj}$ with $V_{sc1}$ grounded while $V_{sc2}$ and $V_{sc3}$ are set as floating nodes.

The circuit model in Fig. 3.9 is constructed with the reference to nodes $V_{sc1}$, $V_{sc2}$ and $V_{sc3}$. The relationships between the three node voltages must be modeled to complete the

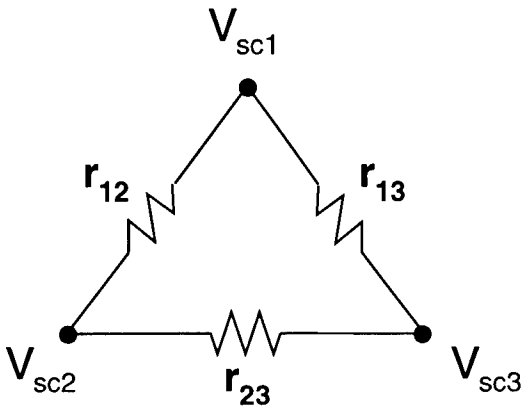


Figure 3.10: The resistor network modeling the relationships between substrate contacts through the silicon substrate.

substrate network. The substrate connection between separate contacts can be represented by a fully connected network of resistors as shown in Fig. 3.10, where $r_{ij}$ is the resistance between contact node $i$ and $j$. Note that $r_{ij}$ is an ordinary two-terminal resistor, not a transfer resistance.

Often the substrate network may be simplified. When the transfer resistance of one branch is significantly larger than another branch, it can be approximated as an open circuit and removed. For instance, when contact $V_{sc1}$ is far from the NMOS transistor (Fig. 3.9). $R^1_{sub}$ may be much larger than one of other substrate resistances. In this case, the branch with reference to $V_{sc1}$ can be eliminated in the substrate network model.

In general, for a circuit layout with $m$ substrate current injection sources and $n$ separate substrate contacts, the substrate network for each device is composed of $n$ parallel branches with each branch containing $m$ series-connected voltage sources. The total number

of elements in the model is, at most, $m^2n$. For most realistic circuit layouts, the substrate network can be simplified. Only a few topside substrate contacts for an I/O cell layout need to be considered in addition to the backside contact (if used).

### 3.2.4 Modeling DRAM circuits

The substrate of a DRAM chip is floating. Most circuit simulators, including iETSIM, encounter convergence problems if floating nodes are included in the circuit description. Thus, an appropriate substrate circuit model must be used for DRAM simulation. When an output driver NMOS experiences positive stress at its drain with respect to a $V_{ss}$ pad,

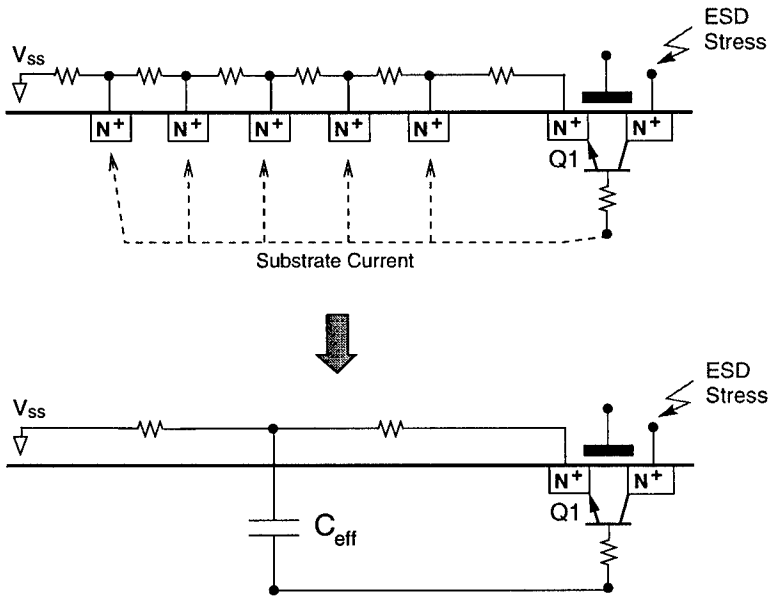


Figure 3.11: Distributed and lumped models for the NMOS impact ionization current flow through the substrate.

the resulting impact ionization current will charge up the coupling capacitance between the $V_{ss}$ bus and silicon substrate as shown in Fig. 3.11. The coupling capacitance consists of junction depletion capacitances and interconnect to substrate capacitances. The distributed

capacitances can be lumped into an effective capacitance $C_{eff}$ as shown in the lumped model in Fig. 3.11.

The floating body of a DRAM chip charged up by the NMOS impact ionization current may forward bias nearby junctions, which need to be modeled as parasitic diodes instead of capacitors. The substrate resistance network modeling the interactions between the NMOS transistor and a junction diode is shown in Fig. 3.12.

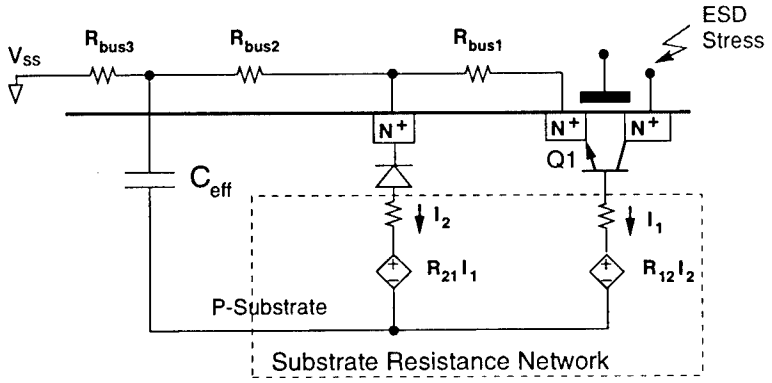


Figure 3.12: The substrate resistance network model for a DRAM circuit.

## 3.3 Substrate Resistance Extraction

We first review the definition of transfer resistance. For a circuit with $m$ injection current sources, $n$ substrate contacts and $p$ monitoring locations (normally $p \leq n$ as shown in Fig. 3.6), $m \times n \times p$ transfer resistances must be calculated using the formula given below.

$$R_{ji}^{k} = V_{ji}^{k} / I_i \tag{3.1}$$

for each $i, j$ and $k$ ($i = 1, \cdots, m$, $j = 1, \cdots, p$ and $k = 1, \cdots, n$), where $I_i$ is the injection current, $V_{ji}^{k}$ is the voltage at location $j$ due to current source $i$ with reference to substrate contact $k$.

The transfer resistance extraction is carried out according to the flow diagram shown in Fig. 3.13. For each source and substrate contact pair, the extraction procedure involves two steps. First, the current distribution on the surface of the injection source is determined. Next, the transfer resistances are extracted for all the monitoring locations. We provide the details of these steps in this section. We also provide details on extraction of the resistors between substrate contacts (see Fig. 3.10).

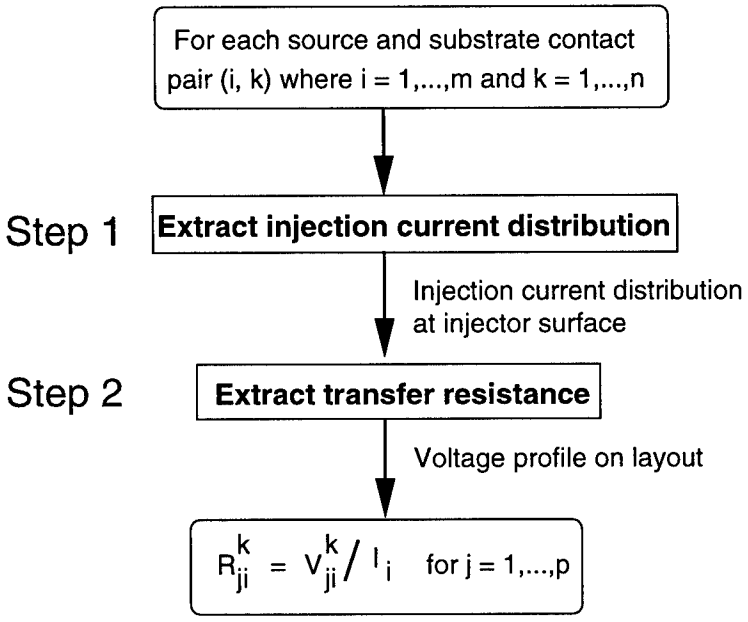


Figure 3.13: The iSREX extraction flow.

### 3.3.1 Transfer resistance extraction

iSREX employs the 3D finite-difference method to extract the transfer resistances. Given a layout structure, e.g., the circuit in Fig. 3.6, we partition the substrate body in the x, y and z directions, forming a network of grids as shown in Fig. 3.14. A 3D resistive network is formed by the grid system. The resistance for each grid is determined by the doping profile

of the substrate. The resistances for the grids inside diffusions or wells are set to infinity

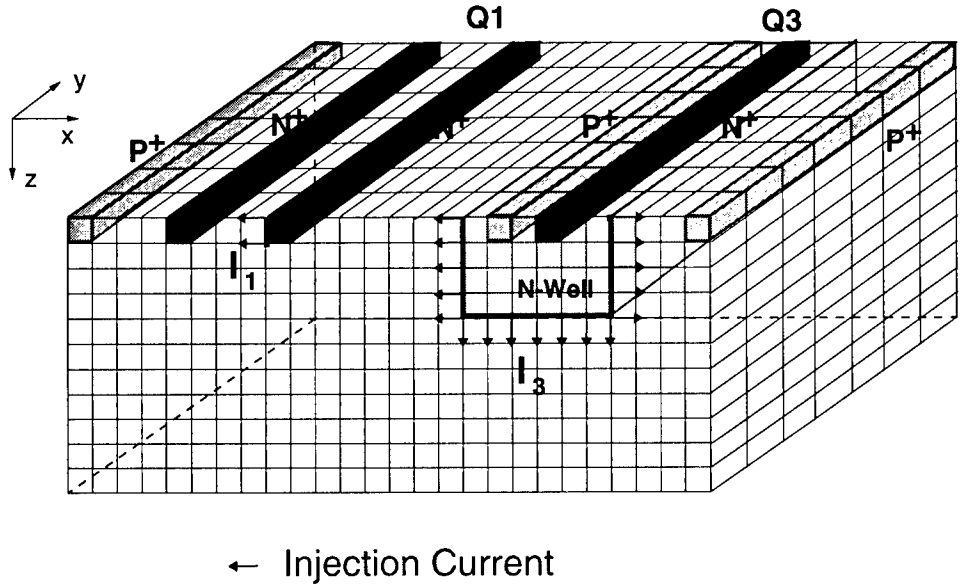


Figure 3.14: Network of grids. ($Q_2$ is not shown here, and the substrate contact is a ring structure surrounding the layout).

(open circuit).

For a specific current source and substrate contact pair, we inject the current from the source according to the surface current distribution obtained from step 1. For a vertical BJT such as a PNP structure, the current is injected from the n-well to substrate. For an NMOS transistor, the impact ionization current is injected from the sidewall of the drain. The referenced substrate contact is set to ground, while other contacts are set floating. A 3D finite difference solver is called to solve the resistive grid system to obtain the voltage profile across the substrate. The inputs to iSREX are layout descriptions ( substrate contacts, active diffusion and well area, current sources and voltage monitoring locations), and process parameters ( vertical doping profile of the substrate, diffusion and well junction depths, etc.). A sample voltage profile is shown in Fig. 3.15.

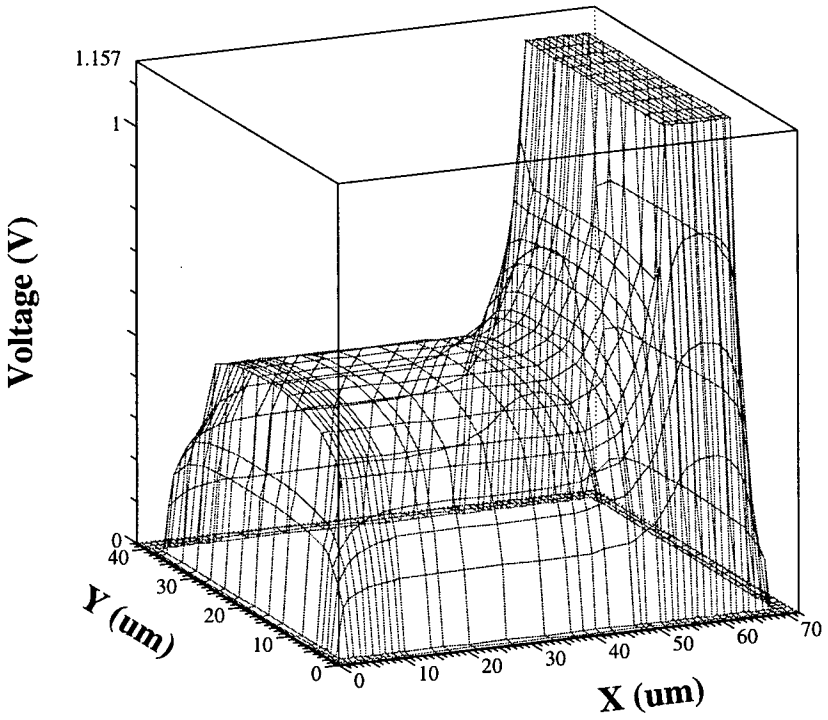


Figure 3.15: The voltage profile at the silicon surface under 10 $mA$ current injection from the vertical BJT $Q_3$. Given a monitoring location such as $Q_1$, the transfer resistance is calculated as the highest voltage around the emitter junction divided by the total injection current. The run time is 269 seconds on a ULTRA1 SUN workstation (including the time to obtain the injection current distribution).

### 3.3.2 Injection current distribution extraction

The voltage profile across the layout strongly depends on the current distribution along the injector surface. Thus, accurate estimation of the injection current distribution is key for accurate extraction of transfer resistances. Considering the case of substrate current injection from a p-n diode in an n-well (Fig. 3.16), we observe that the current will tend to flow along the lowest resistance paths and the distribution at the injector surface is primarily determined by the relative location of the substrate contact. In a previous work [33], an analytical 2D model for the transfer resistance was developed using a fitting distribution parameter (extracted from device simulation results) to model the current distribution along the n-well sidewall and bottom.

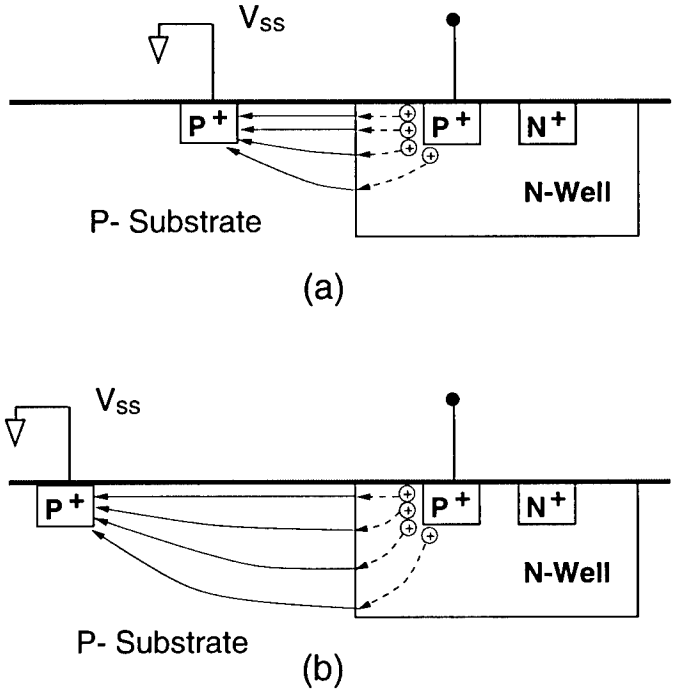


Figure 3.16: The different current flow due to different substrate contact locations.

In iSREX, we use a novel method to determine the injection current distribution. Given

that the injector surface is an equipotential, the current injection distribution from the n-well can be estimated using the finite difference method as follows. We apply the same grid system shown in Fig. 3.14. Assuming that the current is injected according to a distribution $\alpha_i$ $(i = 1, \cdots, n)$ where $n$ is the total number of grid points on the injector surface, the following equations must hold.

$$\begin{bmatrix} R_{11} & R_{12} & \cdots & R_{1n} \\ R_{21} & R_{22} & \cdots & R_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ R_{n1} & R_{n2} & \cdots & R_{nn} \end{bmatrix} \begin{bmatrix} \alpha_1 I \\ \alpha_2 I \\ \vdots \\ \alpha_n I \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix} \tag{3.2}$$

$$V_1 = V_2 = \cdots = V_n = V$$

$$\alpha_1 + \alpha_2 + \cdots + \alpha_n = 1$$

where $R_{ij}$ is the transfer resistance of grid point $i$ due to the current injection at grid point $j$, and $V_i$ is the potential at the injection point $i$. Of course, all the $V_i$'s must be equal. Note that point $i$ and $j$ reside on the injector surface, and $R_{ij}$ is the transfer resistance due to current injection at a single point. $R_{ij}$ can be extracted by the finite difference solver by following the procedure described in section 3.1. Assuming unit injection current $I = 1$, Eq. (3.2) can be rewritten as

$$\begin{bmatrix} R_{11} & R_{12} & \cdots & R_{1n} & -1 \\ R_{21} & R_{22} & \cdots & R_{2n} & -1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ R_{n1} & R_{n2} & \cdots & R_{nn} & -1 \\ 1 & 1 & \cdots & 1 & 0 \end{bmatrix} \begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \vdots \\ \alpha_n \\ V \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 1 \end{bmatrix} \tag{3.3}$$

We can solve the $n+1$ equations for the $n+1$ unknowns which are $\alpha_i$ $(i = 1, \cdots, n)$ and $V$.

Although a vertical BJT was used to illustrate the procedure, the method applies for other devices.

### 3.3.3 Two-terminal resistor extraction

The resistance extraction for two-terminal resistors such as shown in Fig. 3.10 is straightforward. For each substrate contact pair, we inject the current into one terminal with the other one grounded. Again we apply the finite difference method to solve the grid system. The resistance is then obtained by dividing the terminal voltage by the injection current.

## 3.4 A Case Study

In the section, we will use an example to demonstrate the usefulness of the substrate resistance network model for layout optimization of protection devices.

The layout of an advanced protection structure utilizing the substrate-triggering concept is shown in Fig. 3.17 (its cross-section is similar to the circuit shown in Fig. 3.6). The circuit consists of a lateral diode to $V_{dd}$ bus and a multifinger NMOS transistor. When the NMOS drain is stressed with positive ESD current with respect to $V_{ss}$, the lateral diode (modeled as a vertical BJT) will first charge up the $V_{dd}$ power line. The BJT collector current will charge up the substrate, and help turn-on the NMOS transistor by reducing its trigger voltage.

The optimum layout of a protection device is critical for its ESD/latchup performance. The critical dimensions of the layout and the default technology parameters are indicated in Fig. 3.17. These critical dimensions must be optimized such that (1) the BJT collector current is able to raise the substrate potential to 0.7 V under positive ESD stress condition, (2) the local substrate potential for each NMOS transistor should be approximately equal so that they behave uniformly, and (3) the circuit must pass the latchup requirement.

In Fig. 3.18, the voltage profile due to the vertical BJT current is drawn along the center

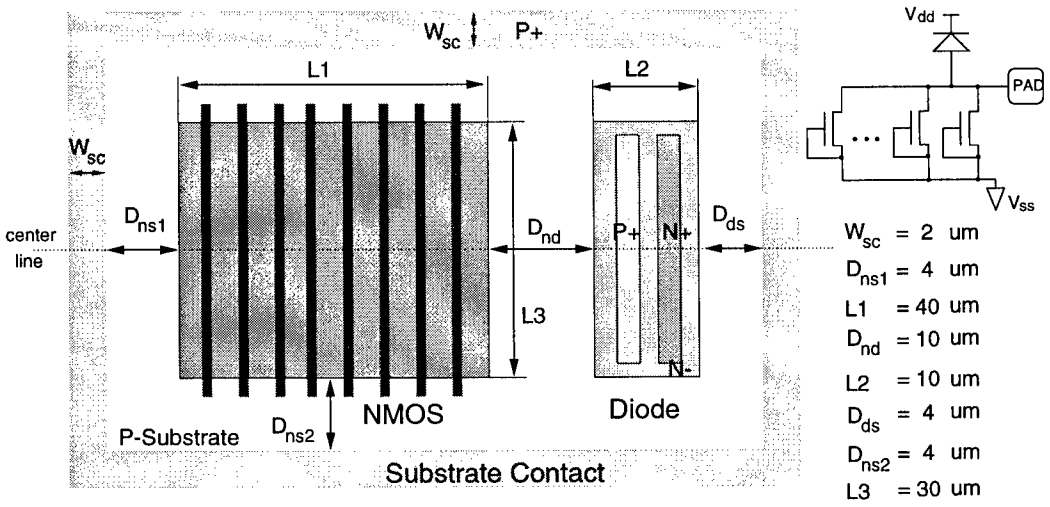


Figure 3.17: The layout of the protection circuit. The critical dimensions are labeled as $D_{nd}$ (NMOS to diode spacing), $D_{ns1}$ and $D_{ns2}$ (NMOS to substrate contact spacings), $D_{ds}$ (diode to substrate contact spacing), and $W_{sc}$ (substrate contact width) and default values are listed. The default technology parameters are $0.2\mu m$ active area depth $T_{act}$, $2\mu m$ well depth $T_{well}$, $6\mu m$ epi thickness $T_{epi}$, $10^{16}\ cm^{-3}$ doping concentration for the epitaxial layer and $10^{20}\ cm^{-3}$ for the p+ substrate.

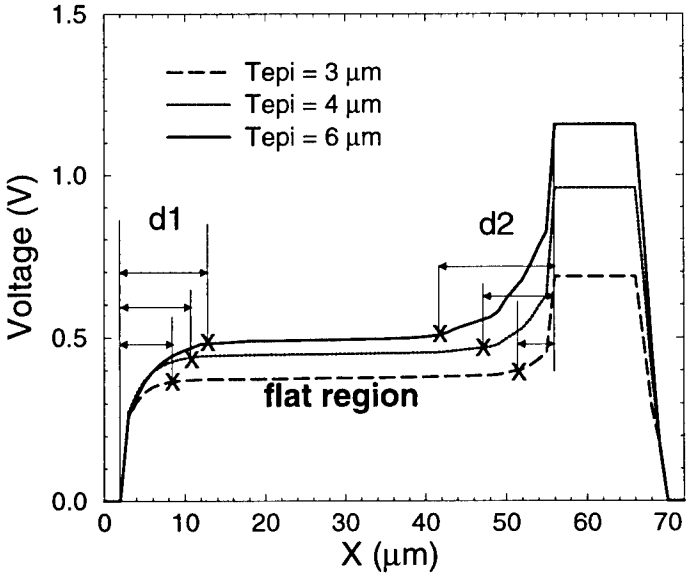


Figure 3.18: The surface voltage profile along the center line under 10 $mA$ current injection from the vertical BJT (lateral diode) for various $T_{epi}$.

line of the layout. There exist three regions in the plot, region d1, a flat region and region d2. It is important that all the NMOS transistors must reside in the flat region so that they can conduct uniform currents. Therefore, $D_{ns1} > d1$ and $D_{nd} > d2$ should be followed as a design rule. Also, the profiles indicate that $d1$ and $d2$ increase as the epitaxial thickness increases.

$D_{ds}$ is another important design parameter. We extract the transfer resistance in the flat region as a function of $D_{ds}$ for various epi thickness (Fig. 3.19). When the substrate contact is close to the diode, i.e. $D_{ds}$ is small, the transfer resistance is greatly reduced. This indicates there is a significant BJT current flowing laterally into the substrate contact on the right side of the layout. When $D_{ds}$ increases, the lateral current will decrease and more will flow from the bottom of n-well, so that it contributes to the transfer resistance in the flat region. The figure indicates that $D_{ds}$ should be at least $T_{epi}$ away from the diode.

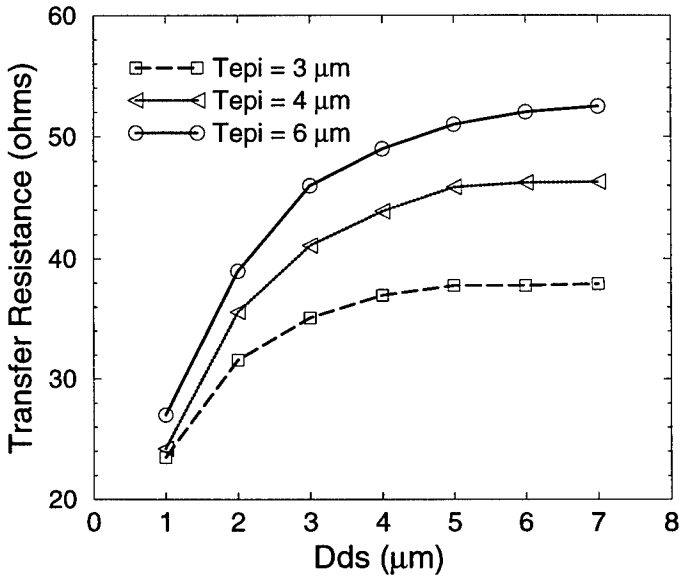


Figure 3.19: The transfer resistance in the flat region (vertical BJT to NMOS transistors) as a function of $D_{s1}$ for various $T_{epi}$.

## 3.5 Summary

In summary, we propose a new substrate resistance network model and its extraction method for circuit-level simulation of CMOS I/O circuits. The substrate network model is general and may be applied to all the devices in CMOS technologies. Furthermore, the substrate model is linked with an I/O layout extractor iLEX which automatically detects parasitic devices and generates simulation input decks.

# Chapter 4

# Semiconductor Resistor Model and Parameter Extractor

A new resistor model has been developed in order to improve the efficiency of simulating I/O circuits using iETSIM (the original model is still available in iETSIM). The new resistor model provides a minimal, simple, and flexible set of physical parameters which can be robustly extracted using RPE, a parameter extractor we have developed. (A detailed explanation of RPE will be provided after the description of the semiconductor resistor model). The model parameters also have a low degree of correlation, which allows a user of iETSIM to optimize a set of parameters by hand if necessary.

Semiconductor resistors are often placed in protection circuits as isolation elements between secondary and primary protection devices. Three distinct regions of operation have been identified which require accurate modeling: low-field (linear) region, high-field (saturation) region, and the breakdown region (see Fig. 4.1). The resistor model will be described in the three following sections.

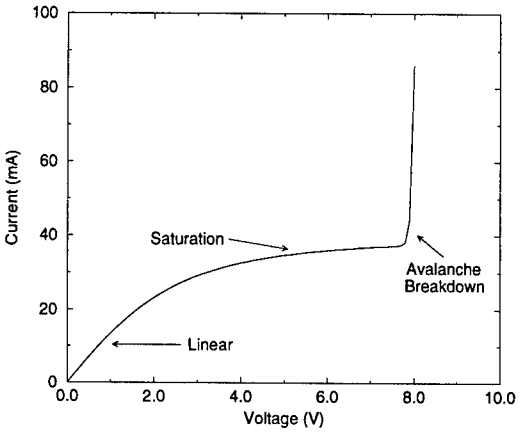


Figure 4.1: Full resistor IV-characteristic.

## 4.1 Resistor Model Description

### 4.1.1 Model derivation

- $\rho$ resistivity $[\Omega - cm]$
- $L$ Drawn Resistor Length $[cm]$
- $\Delta L$ Length correction value $[cm]$
- $W$ Drawn Width of the resistor $[cm]$
- $\Delta W$ Width correction value $[cm]$
- $X_j$ Junction depth of the resistor $[cm]$
- $q$ Charge of an electron $[C]$
- $\mu_{eff}$ Effective carrier mobility $[\frac{cm^2}{V-s}]$

- $\mu_o$ Low-field carrier mobility $[\frac{cm^2}{V-s}]$
- $N$ Majority Carrier concentration $[cm^{-3}]$
- $n_i$ Intrinsic Carrier concentration $[cm^{-3}]$
- $E$ Electric field $[V/cm]$
- $E_{sat}$ Saturation field value $[V/cm]$
- $\beta$ Fitting parameter $[1.0 \leq \beta \leq 2.0]$
- $v_{drift}$ Effective drift velocity of carriers $[cm/s]$
- $v_{sat_o}$ Velocity saturation value $[cm/s]$
- $g_o$ Low-field conductance $[mho]$
- $V$ Applied voltage across resistor $[volts]$

$$I = WX_j(N + n_i)v_{drift} \tag{4.1}$$

We use the field relation found in [37], [38], [39] which has seen substantial verification:

$$v_{drift} = \mu_{eff}E = \frac{\mu_o E}{\left[1 + \left(\frac{E}{E_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{4.2}$$

In this equation, $v_{drift}$ refers to an effective value of the distribution of drift velocities of the carriers. Also, $E$ refers to an effective field value since the electric field distribution across the length of the resistor is constant only in the low-field regime. A linear field profile

is assumed in the device. Thus, $E = \frac{V}{L_{eff}}$ where $L_{eff} = (L - \Delta L)$. $L$ is the drawn resistor length. The saturation field is defined as $E_{sat} = \frac{v_{sat_o}}{\mu_o}$.

Now, substituting for $v_{drift}$:

$$I = W(N + n_i)\frac{\mu_o E}{\left[1 + \left(\frac{E}{E_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{4.3}$$

Re-writing the current in terms of the conductance ($g_o$):

$$I = \frac{g_o V}{\left[1 + \left(\frac{E}{E_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{4.4}$$

where $g_o$ is

$$g_o = \frac{q\mu_o(N + n_i)X_j W_{eff}}{L_{eff}} \tag{4.5}$$

In order to obtain a low-field conductance value which is independent of length and width, we redefine the conductance as:

$$g_o = q\mu_o(N + n_i)X_j \tag{4.6}$$

Finally, we obtain the complete resistor model equation:

$$I = \frac{g_o(W - \Delta W)V}{(L - \Delta L)\left[1 + \left(\frac{V}{(L-\Delta L)E_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{4.7}$$

Thus, this simple model is capable of describing both the low-field and high-field regions of typical semiconductor resistors.

## 4.2 Breakdown Model Description

In order to provide an accurate and simple method of modeling the high current regime of semiconductor resistors, we chose to utilize macromodeling techniques instead of conventional physical modeling methods.

The typical resistor IV-characteristic is displayed in Fig. 4.1. As shown, the resistor breaks down at voltages commonly found in typical ESD circuits.

This breakdown phenomenon can efficiently and accurately be modeled using an electric field value at breakdown. By specifying the electric field at breakdown, the resistor breakdown voltage scales appropriately based on the resistor length. The validity of describing breakdown with an electric field value is demonstrated in Fig. 4.2.

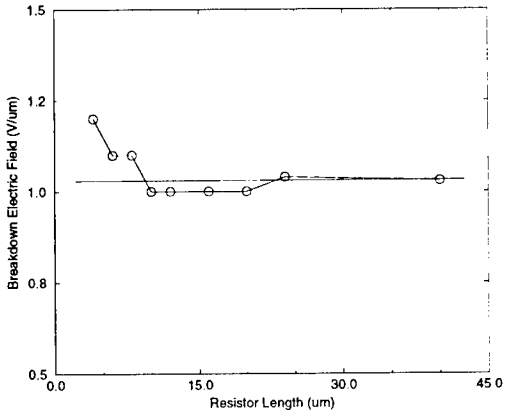


Figure 4.2: Breakdown field is nearly independent of resistor length.

Breakdown is represented by using a diode placed in parallel with the resistor (see

Fig. 4.3). The turn-on voltage (typically 0.7 volts for physical diodes) is altered to produce the correct breakdown voltage.

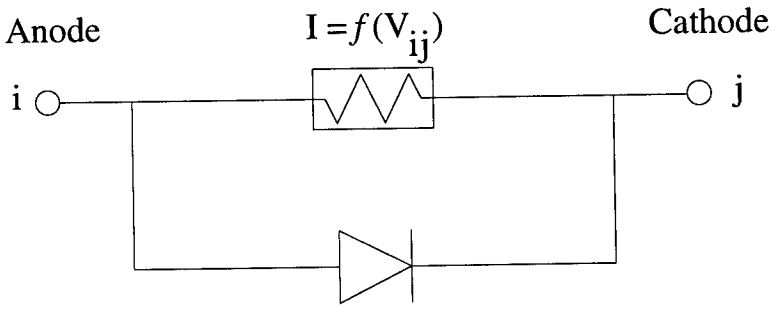


Figure 4.3: Resistor model with additional breakdown circuit modeling included.

## 4.3 Thermal Model Description

This resistor model is intended to be used in conjunction with iETSIM and therefore thermal effects must be accounted for. Therefore, modified expressions for temperature dependent parameters must be used. These parameters include the carrier concentration, mobility, and velocity saturation.

The intrinsic carrier concentration temperature dependence is given by

$$n_i(T) = n_{io}\left(\frac{T}{T_o}\right)^{1.5} \exp\left(\frac{E_g(T_o)}{2kT_o} - \frac{E_g(T)}{2kT}\right) \tag{4.8}$$

where $n_{io}$ is the intrinsic carrier concentration evaluated at $T_o$ ($n_{io}$=1.5 $\times$ $10^{10}$cm$^{-3}$ at 300 K). The temperature dependence of the bandgap energy is given by

$$E_g(T) = E_g(0) - \frac{E_{g\alpha}T^2}{T + E_{g\beta}} \tag{4.9}$$

where $E_{g\alpha}$ and $E_{g\beta}$ are material constants and T again is the temperature ([35], [42]).

The temperature dependence of $v_{sat}$ (cm/s) is described by a well-established empirical model [37]:

$$v_{sat}(T) = v_{sat_o}\left(\frac{T}{300}\right)^{-0.87} \tag{4.10}$$

The temperature dependence for mobility as reported in [44] is employed (default is $\alpha_n = 2.6$).

$$\mu_n(T) = \mu_o\left(\frac{T}{300}\right)^{\alpha_n} \tag{4.11}$$

Thus, $E_{sat}$ will have the following temperature dependence:

$$E_{sat}(T) = \frac{v_{sat}(T)}{\mu(T)} \tag{4.12}$$

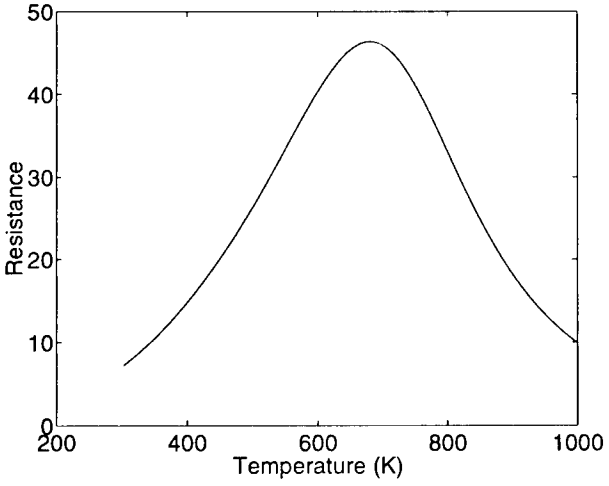


Figure 4.4: Temperature dependence of the resistor.

A plot of the resistance as a function of temperature is show in Fig. 4.4. At low temperatures, the behavior is dominated by the temperature dependence of mobility: at high temperatures, the behavior is dominated by the termperature dependence of the intrinsic carrier concentration.

## 4.4 Introduction to RPE

RPE is has been developed at the University of Illinois in order to provide a tool to extract model parameters for semiconductor resistors which will be used to run simulations using iETSIM.

The two most important capabilities RPE offers are:

(1) Automated IV tests on semiconductor resistor structures.

(2) Device model parameter extraction and optimization in order to achieve an optimal fit between the model and the measured data.

RPE is the acronym for **R**esistor **P**arameter **E**xtractor. This program has been coded in Visual Basic and is intended to be used in the MS-Windows environment. RPE tool enables a user to make automated IV-measurements of semiconductor resistors using an HP4145 semiconductor parameter analyzer (Model A or B).

RPE is also used to extract parameters for the resistor model detailed in Section 4.1. RPE can be used to extract model parameters for either single or multiple data sets. The extracted parameters can then be used to accurately model resistor IV behavior in the circuit simulation tool iETSIM

## 4.5 Parameter Optimization

RPE can be used to obtain an optimal set of parameters over multiple data sets. The parameters required to accurately model several data sets include: $g_o$, $E_{sat}$, $\Delta L$, and $\Delta W$.

The low-field conductance is extracted by finding the slope of the tangent line where the resistor IV curve is linear (see Fig. 4.5). The electric-field saturation value ($E_{sat}$) is extracted by obtaining an optimal fit between the data and the model.

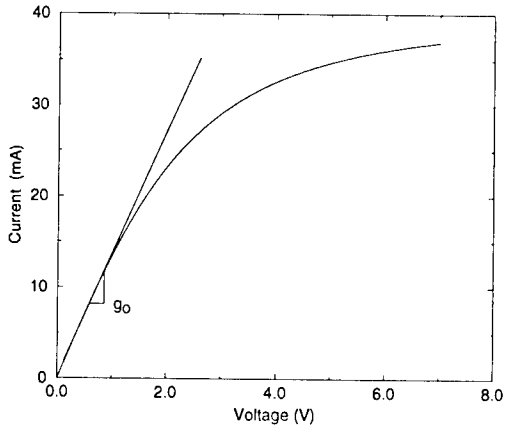


Figure 4.5: Graph demonstrating extraction of the low-field conductance.

The parameters $\Delta L$ and $\Delta W$ are used to model the difference between the electrical length/width and physical length/width of the measured resistors.

The user can also graph the data sets with the most recently reported set of parameters at any time during the parameter optimization period. (see Figs. 4.6 and 4.7).

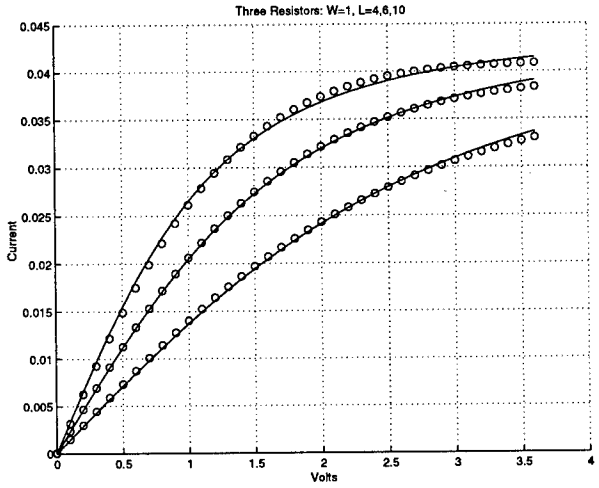


Figure 4.6: Graph of multiple data sets and resulting calculated IV models obtained by the RPE optimizer.

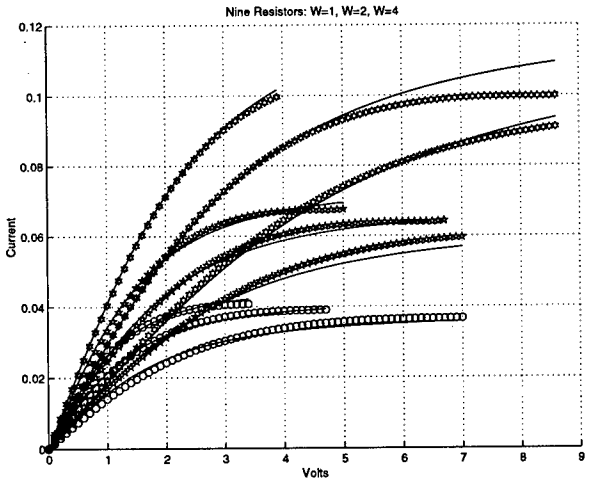


Figure 4.7: Graph of multiple data sets and resulting calculated IV models obtained by the RPE optimizer.

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# Chapter 5

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